



File Name	Specification For 2.66" EPD	Module Number	E0266A146
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Specification For 2.66"EPD

Model NO.: E0266A146

Product VER: A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver, if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By



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Version	Content	Date	Producer
A0	New release	2023/3/15	Eddie. Huang



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1. General Description

E0266A146 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design. The 2.66" active area contains 152*296 pixels, and has 2-bit B/W/R/Y full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2. Features

- 152*296 pixels display
- High contrast
High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/ built-in temperature sensor

3. Application

Electronic Shelf Label System

4. Mechanical Specifications

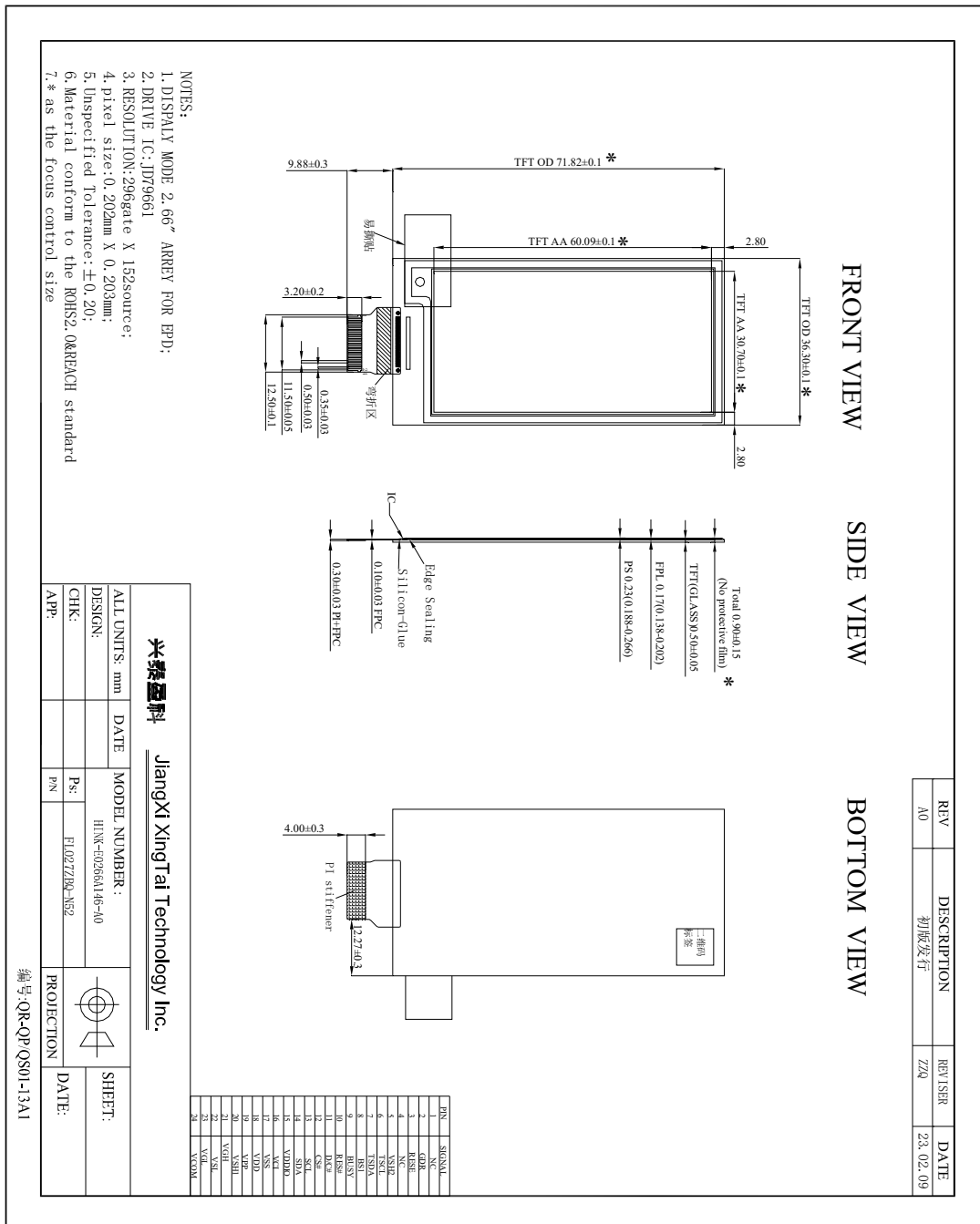
Parameter	Specifications	Unit	Remark
Screen Size	2.66	Inch	
Display Resolution	152(H)×296(V)	Pixel	Dpi:125
Active Area	30.7(H)×60.09(V)	mm	



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Pixel Pitch	0.202×0.203	mm	
Pixel Configuration	Rectangle		
Outline Dimension	36.3(H)×71.82(V) ×0.95(D)	mm	Without masking film
Weight	3.6±0.5	g	

5. Mechanical Drawing of EPD module





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6. Input/output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VSH2	Positive Source driving voltage	
6	TSCL	I ² C Interface to digital temperature sensor Clock pin	Suggest to connect GND if not being used
7	TSDA	I ² C Interface to digital temperature sensor Data pin.	Suggest to connect GND if not being used
8	BS1	Bus selection pin	Note 6-5
9	BUSY	Busy state output pin	Note 6-4
10	RES #	Reset signal input.	Note 6-3
11	D/C #	Data /Command control pin	Note 6-2
12	CS #	The chip select input connecting to the MCU.	Note 6-1
13	SCL	Serial clock pin for interface.	
14	SDA	Serial data pin for interface.	
15	VDDIO	Power input pin for the Interface.	
16	VCI	Power Supply pin for the chip	
17	VSS	Ground (Digital)	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH1	Positive Source driving voltage	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	Negative Source driving voltage	
23	VGL	Power Supply pin for Negative Gate driving voltage, VCOM and VSL	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CS# is pulled LOW.



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Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled LOW, the data will be interpreted as command.

Note 6-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is High, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin High when the driver IC is working such as:

- Outputting display waveform;
- Communicating with digital temperature sensor

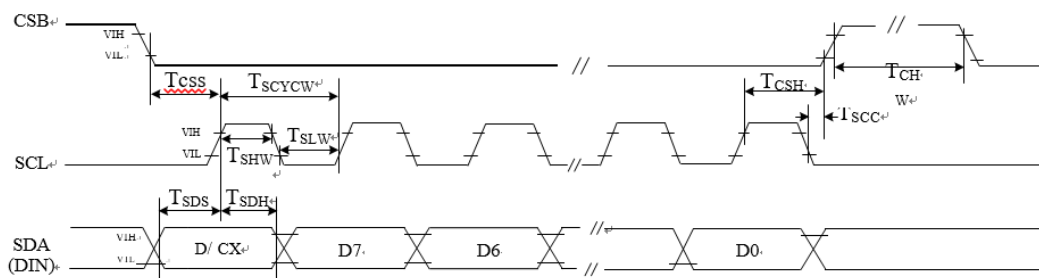
Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected.

7. MCU Interface

E0266A146 use the 3-wire/4-wire serial port as communication interface for all the function and command setting. 3-wire/4-wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-wire/4-wire bus itself.

Under read mode, 3-wire/4-wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-wire/4-wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”

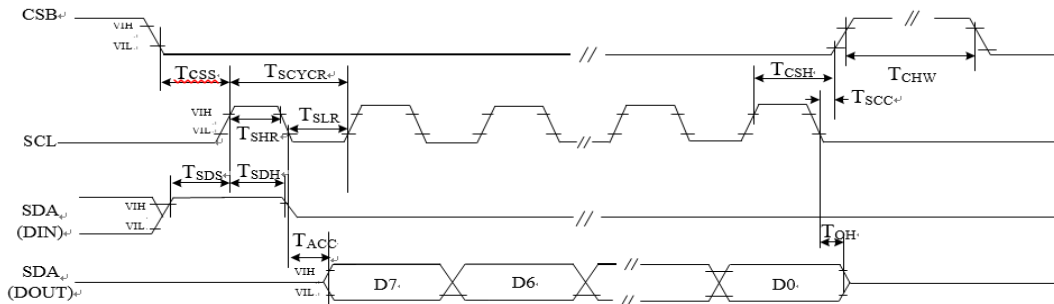
7.1 “3-Wire” Serial Port Interface



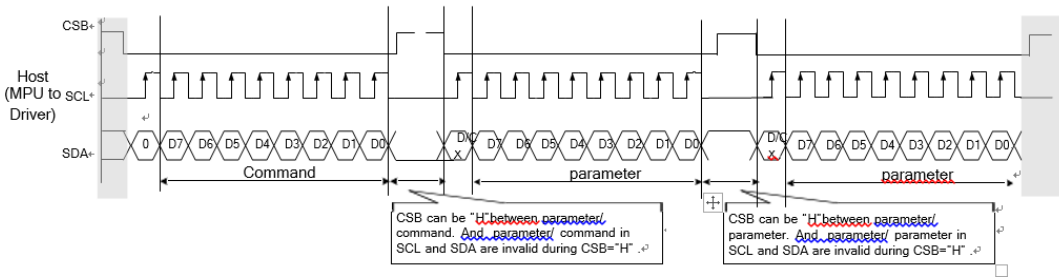
3 pin serial interface characteristics (write mode)



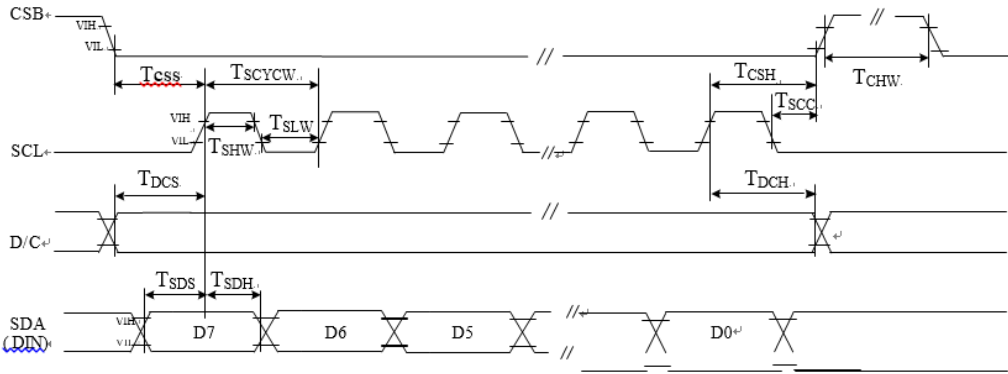
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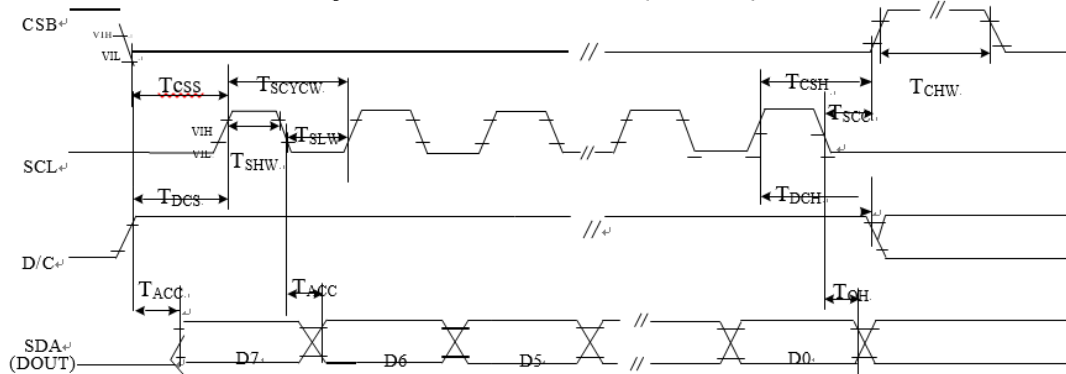
3 pin serial interface characteristics (read mode)



7.2 "4-Wire" Serial Port Interface



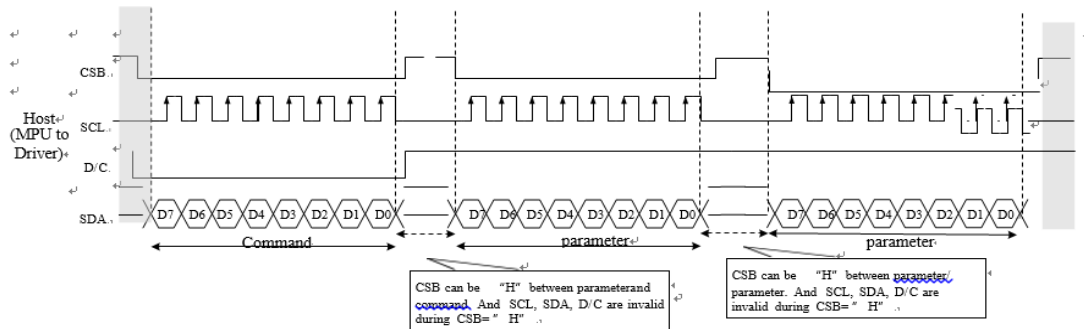
4 pin serial interface characteristics (write mode)



4 pin serial interface characteristics (read mode)



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8. Command Table

8.1 Register Table

Following table list all the SPI control registers and bit name definition for JD79661AA.

Refer to the next section for detail register function description.

Address	command	Bit										
		R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
R00H	Panel setting (PSR)	W	0	0	0	0	0	0	0	0	0	00H
		W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
		W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h
R01H	Power setting (PWR)	W	0	0	0	0	0	0	0	0	1	01H
		W	1	-	-	-	-	V_MODE	VSC_EN	VDS_EN	VDG_EN	07h
		W	1	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
		W	1	-	VSPL_0[6]	VSPL_0[5]	VSPL_0[4]	VSPL_0[3]	VSPL_0[2]	VSPL_0[1]	VSPL_0[0]	00h
		W	1	-	VSP_1[6]	VSP_1 [5]	VSP_1 [4]	VSP_1 [3]	VSP_1 [2]	VSP_1 [1]	VSP_1 [0]	00h
		W	1	-	VSN_1[6]	VSN_1[5]	VSN_1[4]	VSN_1[3]	VSN_1[2]	VSN_1[1]	VSN_1[0]	00h
		W	1	-	VSPL_1[6]	VSPL_1[5]	VSPL_1[4]	VSPL_1[3]	VSPL_1[2]	VSPL_1[1]	VSPL_1[0]	00h
R02H	Power OFF(POF)	W	0	0	0	0	0	0	0	1	0	02H
		W	1	-	-	-	-	-	-	-	EDSE	00h
R03H	Power off Sequence Setting(PFS)	W	0	0	0	0	0	0	0	1	1	03H
		W	1	-	-	-	T_VDPG_OFF[1:0]	-	-	-	T_VDS_OFF[1:0]	00h
		W	1	-	-	-	VGP_LEN[3:0]	-	-	-	VGP_EXT[3:0]	54
		W	1	-	-	-	XON_DLY	-	-	-	XON_LEN	44
R04H	Power ON (PON)	W	0	0	0	0	0	0	1	0	0	04H
		W	0	0	0	0	0	0	1	1	0	06H
		W	1	-	-	-	-	-	PHB_SFT[1:0]	-	PHA_SFT[1:0]	00h
		W	1	-	-	-	-	-	PHA_ON[5:0]	-	-	02h
		W	1	-	-	-	-	-	PHA_OFF[5:0]	-	-	07h



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R06H	Booster Soft Start (BTST)	W	1	-	-	PHB_ON[5:0]						02h
		W	1	-	-	PHB_OFF[5:0]						07h
		W	1	-	-	PHC_ON[5:0]						02h
		W	1	-	-	PHC_OFF[5:0]						07h
R07H	Deep Sleep(DSLP)	W	0	0	0	0	0	0	1	1	1	07H
		W	1	1	0	1	0	0	1	0	1	A5h
R10H	Data Start transmission (DTM)	W	0	0	0	0	1	0	0	0	0	10H
		W	1	#	#	#	#	#	#	#	#	00H
R11H	Data Stop (DSP)	W	0	0	0	0	1	0	0	0	1	11H
		R	1	Data_flag	-	-	-	-	-	-	-	-
R12H	Display Refresh (DRF)	W	0	0	0	0	1	0	0	1	0	12H
		W	1	-	-	-	-	-	-	-	-	AC/DC
R17H	Auto sequence (AUTO)	W	0	0	0	0	1	0	1	1	1	17H
		W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h
R20H	LUT0	W	0	0	0	1	0	0	0	0	0	20H
		W	1	#	#	#	#	#	#	#	#	00h
R30H	PLL control (PLL)	W	0	0	0	1	1	0	0	0	0	30H
		W	1	-	-	-	-	Dyna	FR[2:0]			02h
R40H	Temperature Sensor Command (TSC)	W	0	0	1	0	0	0	0	0	0	40H
		R	1	D10/TS[7]	D9/TS[7]	D8/TS[6]	D7/TS[5]	D6/TS[4]	D5/TS[3]	D4/TS[2]	D3/TS[1]	--
		R	1	D2/TS[9]	D1/TS[8]	D0	-	-	-	-	-	--
R41H	Temperature Sensor Calibration (TSE)	W	0	0	1	0	0	0	0	0	1	41H
		W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h
R42H	Temperature Sensor Write (TSW)	W	0	0	1	0	0	0	0	1	0	42H
		W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
		W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h

R43H	Temperature Sensor Read (TSR)	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h
		W	0	0	1	0	0	0	0	1	1	43H
		R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	--
R44H	Panel Glass Check (PGC)	W	0	0	1	0	0	0	1	0	0	44H
		R	1	-	-	-	-	-	-	-	PSTA	-
R50H	VCOM and DATA interval setting (CDD)	W	0	0	1	0	1	0	0	0	0	50H
		W	1	VBDI[2]	VBDI[1]	VBDI[0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h
R51H	Lower Power Detection (LPD)	W	0	0	1	0	1	0	0	0	1	51H
		R	1	-	-	-	-	-	-	-	LPD	--
	TCON setting	W	0	0	1	1	0	0	0	0	0	60H
		W	1	-	-	S2G[5]	S2G[4]	S2G[3]	S2G[2]	S2G[1]	S2G[0]	02h



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R60H	(TCON)	W	1	-	-	G2SF51	G2SF41	G2SF31	G2SF21	G2SF11	G2SF01	02h
R61H	Resolution setting(TRES)	W	0	0	1	1	0	0	0	0	1	61H
		W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRES(8)	VRES(0)	00h
		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h
R65H	Gate/Source Start Setting(GSST)	W	0	0	1	1	0	0	1	0	1	65H
		W	1	-	-	-	-	-	-	S_start(9)	S_start(8)	00h
		W	1	S_start(7)	S_start(6)	S_start(5)	S_start(4)	S_start(3)	S_start(2)	0	0	00h
		W	1	-	-	-	-	-	-	G_start(9)	G_start(8)	00h
		W	1	G_start(7)	G_start(6)	G_start(5)	G_start(4)	G_start(3)	G_start(2)	G_start(1)	G_start(0)	00h
R70H	REVISION (REV)	W	0	0	1	1	1	0	0	0	0	70H
		R	1	0	0	0	0	0	0	1	1	03h
		R	1	0	0	0	0	0	0	0	1	02h
		R	1	0	0	0	0	0	0	0	1	01h
R71H	Status register(FLG)	W	0	0	1	1	1	0	0	0	1	71H
		R	1	AMV_Busy	PTI_flg	I ² C_ERR	I ² C_	-	PON	POF	BUSY_N	--
		R	1	-	-	-	-	-	LV_ST	BT_OK	ED_Busy	--
R80H	Auto Measure Vcom (AMV)	W	0	1	0	0	0	0	0	0	0	80H
		W	1	PI1	PI0	AMVTI11	AMVTI01	XON	AMVS	AMV	AMVE	00h
R81H	Vcom Value (VV)	W	0	1	0	0	0	0	0	0	1	81H
		R	1	-	VVI[6]	VVI[5]	VVI[4]	VVI[3]	VVI[2]	VVI[1]	VVI[0]	--
R82H	Vcom_DC Setting (VDCS)	W	0	1	0	0	0	0	0	1	0	82H
		W	1	MTP_VCM	VDCS[6]	VDCS[5]	VDCS[4]	VDCS[3]	VDCS[2]	VDCS[1]	VDCS[0]	00h
R83H	Partial Window (PTLW)	W	0	1	0	0	0	0	0	1	1	83H
		W	1	-	-	-	-	-	-	HRST(9)	HRST(8)	00h
		W	1	HRST(7)	HRST(6)	HRST(5)	HRST(4)	HRST(3)	HRST(2)	0	0	00h
		W	1	-	-	-	-	-	-	HRED(9)	HRED(8)	00h
		W	1	HRED(7)	HRED(6)	HRED(5)	HRED(4)	HRED(3)	HRED(2)	0	0	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	VRST(9)	VRST(8)	00h
		W	1	VRST(7)	VRST(6)	VRST(5)	VRST(4)	VRST(3)	VRST(2)	VRST(1)	VRST(0)	00h
		W	1	-	-	-	-	-	-	-	PMOD	00h
R84H	Program	W	0	1	0	0	0	0	0	0	00h	
R84H	Active	W	0	1	0	0	0	0	0	0	00h	
R92H	Read MTP data (MTP)	W	0	1	0	0	1	0	0	1	0	92H
		R	1	#	#	#	#	#	#	#	#	-
R93H	Read SRAM data (SRAM)	W	0	1	0	0	1	0	0	1	1	93H
		R	1	#	#	#	#	#	#	#	#	-
R9EH	REVISION2 (REV2)	W	0	1	0	0	1	1	1	1	0	9EH
		R	1	0	0	0	0	0	0	0	1	01h

		W	0	1	0	0	1	1	1	1	1	9FH
--	--	---	---	---	---	---	---	---	---	---	---	-----



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RA0H	Read MTP Reserved	R	1	#	#	#	#	#	#	#	#	-	
RA0H	Load MTP	W	0	1	0	1	0	0	0	0	0	A0H	
RA1H	Read LUT RAM register(RLUT)	W	0	1	0	1	0	0	0	0	1	A1H	
		R	1	#	#	#	#	#	#	#	#	-	
RA2H	MTP Program Config Register(PGM_CFG)	W	0	1	0	1	0	0	0	1	0	A2H	
		W	1	-	-	-	VMTPSE	-	-	-	-	-	00h
		W	1	PGM_SADDR[15:8]									00h
		W	1	PGM_SADDR[7:0]									00h
		W	1	PGM_DSIZE[15:8]									15h
		W	1	PGM_DSIZE[7:0]									E0h
RA3H	MTP Program Status Register(PGM_STAT)	W	0	1	0	1	0	0	0	1	1	A3H	
		R	1	-	-	-	-	-	-	PGM_VER	PGM_EXE	00h	
RA5H	Load LUT from RAM	W	0	1	0	1	0	0	1	0	1	A5H	
RE0H	CASCADE setting (CCSET)	W	0	1	1	1	0	0	0	0	0	E0H	
		W	1	-	-	-	-	-	-	TSFIX	CCEIN	00h	
RE3H	Power saving(PWS)	W	0	1	1	1	0	0	0	1	1	E3H	
		W	1	VCOM_	VCOM_	VCOM_	VCOM_	SD_W[3]	SD_W[2]	SD_W[2]	SD_W[0]	00h	
RE4H	LVD voltage Select(LVSEL)	W	0	1	1	1	0	0	1	0	0	E4H	
		W	1	-	-	-	-	-	-	LVD_S	LVD_S	03h	
RE6H	Force Temperature(TSSET)	W	0	1	1	1	0	0	1	1	0	E6H	
		W	1	TS_SET[7]	TS_SET[6]	TS_SET[5]	TS_SET[4]	TS_SET[3]	TS_SET[2]	TS_SET[1]	TS_SET[0]	03h	
RE7H	Power Switch Time(PST)	W	0	1	1	1	0	0	1	1	1	E7H	
		W	1	-	-	PSTI[3:0]				PST[1:0]		1Ch	
RE8H	CRC status register(CRC_STAT)	W	0	0	1	1	0	1	0	0	0	E8H	
		R	1	-	-	-	-	-	-	-	CRC_STA	00h	
		R	1	Chk_CRC[7:0]									00h
RE9H	CRC Enable register(CRC_EN)	R	1	MTP_CRC[7:0]									00h
		W	0	1	1	1	0	1	0	0	1	E9H	
		W	1	-	-	-	-	-	-	-	CRC_IGN	00h	

8.2 Register Description

R/W: 0: Write Cycle 1:Read Cycle

D/CX:0: Command/1:Data

D7~D0:-:Don't Care

8.2.1 R00H (PSR): Panel setting Register

R00H	Bit										
	Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0



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PSR	W	0	0	0	0	0	0	0	0	0	00H
1 st Parameter	W	1	RES[1]	RES[0]	PST_MODE	-	UD	SHL	SHD_N	RST_N	0Fh
2 nd Parameter	W	1	LUT_EN	-	FOPT	VCMZ	TS_AUTO	TIEG	NORG	VC_LUTZ	09h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	1 st parameter										
	Bit	Name	Description								
	0	RST_N	RST_N function 1: no effect. (default) 0: Booster OFF, Register data are set to their default values, and Source/Boder/Vcom: floating								
	1	SHD_N	SHD_N function 0: Booster OFF, register data are kept, and Source/Boder/Vcom are kept 0V or floating 1: Booster on. (default)								
	2	SHL	SHL function 0: Shift left: First data=S _n →S _{n-1} →...→S ₂ → Last data=S ₁ 1: Shift right: First data=S ₁ →S ₂ →...→S _{n-1} → Last data=S _n . (default)								
	3	UD	UD function 0: Scan down: First line=G _n →G _{n-1} →...→G ₂ → Last line=G ₁ . 1: Scan up; First line=G ₁ →G ₂ →...→G _{n-1} → Last line=G _n . (default)								
	5	PST_MODE	Power switch operation mode 0: Power switching time in the period of frame scanning. (default) 1: Power switching time in the external period before frame scanning.								
	7-6	RES[1,0]	Resolution setting 00: Display resolution is 176x296 (default) 01: Display resolution is 128x296 10: Display resolution is 128x250 11: Display resolution is 112x204								
	2 nd parameter										
	Bit	Name	Description								
	0	VC_LUTZ	VCOM status function 0: No effect 1: After refreshing display, the output of VCOM is set to floating automatically (default)								
	1	NORG	VCOM status function 0: No effect (default) 1: After refreshing display, VCOM is tied to GND before power off								
	2	TIEG	VGN power off status function 0: No effect (default) 1: Power off, VGN will be tied to GND								



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3	TS_AUTO	Temperature sensing will be activated automatically one time 0 : Before enabling booster, Temperature Sensor will be activated automatically one time. 1 : When RST_N low to high, Temperature Sensor will be activated automatically one time. (default)
4	VCMZ	VCOM status function 0 : No effect (default) 1 : VCOM is always floating
5	FOPT	FOPT function 0: Scan 1 frame after waveform finished(default) 1: No scan after waveform finished and switch the source channel output to Hiz.
7	LUT_EN	LUT selection setting 0 : Using LUT from MTP(default) 1 : Using LUT from register
<p>Priority of VCOM setting: VCMZ > NORG > FOPT > VC_LUTZ</p> <p>FOPT setting is part of refreshing display.</p> <p>FOPT: Power off floating.</p> <p>Notes:</p> <ol style="list-style-type: none"> Non-select gate line keep at VGN for DSP/DRF and AMV Dummy source line follow LUTC for DSP/DRF When SHD_N become low, DCDC will turn off. Register and SRAM data will keep until VDD turn off. SD output and VCOM will base on previous condition . It may have two condition: 0V or floating. When RST_N become low, driver will reset. All register will reset to default value. All of the driver's functions will disable. Source/Gate/Border/VCOM will be released to floating 		
Restriction		

8.2.2 R01H (PWR): Power setting Register

R01H	Bit										Code	
	Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1		D0
PWR	W	0	0	0	0	0	0	0	0	0	1	01h
1 st Parameter	W	1	-	-	-	-	-	V_MODE	VSC_EN	VDS_EN	VDG_EN	07h
2 nd Parameter	W	1	-	-	-	-	-	-	-	VGPN [1]	VGPN [0]	00h
3 rd Parameter	W	1	-	VSPL_0 [6:0]								00h



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4 th Parameter	W	1	-	VSP_1 [6:0]	00h
5 th Parameter	W	1	-	VSN_1 [6:0]	00h
6 th Parameter	W	1	-	VSPL_1 [6:0]	00h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command defines as :		
	1 st Parameter:		
	Bit	Name	Description
	0	VDG_EN	Gate power selection. 0 : External gate power from VGP/VGN pins. 1 : Internal DCDC function for generate VGP/VGN. (default)
	1	VDS_EN	Source power selection. 0 : External source power from VSP/VSN pins. 1 : Internal regulator function for generate VSP/VSN (default)
	2	VSC_EN	Source LV power selection. 0 : External source power from VSPL pins. 1 : Internal regulator function for generate VSPL (default)
	3	V_MODE	Source Power switching mode. 0: Mode0(default) 1: Mode1
	2nd Parameter:		
	Bit	Name	Description
	1-0	VGPN	VGPN Voltage Level. 00: VGP=20 v, VGN=-20v (default) 01: VGP=17 v, VGN=-17v 10: VGP=15 v, VGN=-15v 11: VGP=10 v, VGN=-10v



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5th Parameter: Internal VSN_1 power selection								
Bit	Name	Description						
		Internal VSN power selection.						
		Voltage(V)	bit [6:0]		Voltage(V)	bit [6:0]		
		00h	-3	0101001	29h	-7.1	1010010	52h -11.2
		01h	-3.1	0101010	2Ah	-7.2	1010011	53h -11.3
		02h	-3.2	0101011	2Bh	-7.3	1010100	54h -11.4
		03h	-3.3	0101100	2Ch	-7.4	1010101	55h -11.5
		04h	-3.4	0101101	2Dh	-7.5	1010110	56h -11.6
		05h	-3.5	0101110	2Eh	-7.6	1010111	57h -11.7
		06h	-3.6	0101111	2Fh	-7.7	1011000	58h -11.8
		07h	-3.7	0110000	30h	-7.8	1011001	59h -11.9
		08h	-3.8	0110001	31h	-7.9	1011010	5Ah -12
		09h	-3.9	0110010	32h	-8	1011011	5Bh -12.1
		0Ah	-4	0110011	33h	-8.1	1011100	5Ch -12.2
		0Bh	-4.1	0110100	34h	-8.2	1011101	5Dh -12.3
		0Ch	-4.2	0110101	35h	-8.3	1011110	5Eh -12.4
		0Dh	-4.3	0110110	36h	-8.4	1011111	5Fh -12.5
		0Eh	-4.4	0110111	37h	-8.5	1100000	60h -12.6
		0Fh	-4.5	0111000	38h	-8.6	1100001	61h -12.7
		10h	-4.6	0111001	39h	-8.7	1100010	62h -12.8
		11h	-4.7	0111010	3Ah	-8.8	1100011	63h -12.9
6-0	VSN_1	12h	-4.8	0111011	3Bh	-8.9	1100100	64h -13
		13h	-4.9	0111100	3Ch	-9	1100101	65h -13.1
		14h	-5	0111101	3Dh	-9.1	1100110	66h -13.2
		15h	-5.1	0111110	3Eh	-9.2	1100111	67h -13.3
		16h	-5.2	0111111	3Fh	-9.3	1101000	68h -13.4
		17h	-5.3	1000000	40h	-9.4	1101001	69h -13.5
		18h	-5.4	1000001	41h	-9.5	1101010	6Ah -13.6
		19h	-5.5	1000010	42h	-9.6	1101011	6Bh -13.7
		1Ah	-5.6	1000011	43h	-9.7	1101100	6Ch -13.8
		1Bh	-5.7	1000100	44h	-9.8	1101101	6Dh -13.9
		1Ch	-5.8	1000101	45h	-9.9	1101110	6Eh -14
		1Dh	-5.9	1000110	46h	-10	1101111	6Fh -14.1
		1Eh	-6	1000111	47h	-10.1	1110000	70h -14.2
		1Fh	-6.1	1001000	48h	-10.2	1110001	71h -14.3
		20h	-6.2	1001001	49h	-10.3	1110010	72h -14.4



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			21h	-6.3	1001010	4Ah	-10.4	1110011	73h	-14.5
			22h	-6.4	1001011	4Bh	-10.5	1110100	74h	-14.6
			23h	-6.5	1001100	4Ch	-10.6	1110101	75h	-14.7
			24h	-6.6	1001101	4Dh	-10.7	1110110	76h	-14.8
			25h	-6.7	1001110	4Eh	-10.8	1110111	77h	-14.9
			26h	-6.8	1001111	4Fh	-10.9	1111000	78h	-15
			27h	-6.9	1010000	50h	-11	other		-15
			28h	-7	1010001	51h	-7.1			

Notes:

- VSP_0/VSN_0 voltage output is ±15 V fixed value.
- When switching Mode0 or Mode1, the voltage output is: Mode0:
VSP_0(+15) / VSN_0 (- 15) / VSPL_0 (+3~+15)
Mode1: VSP_1(+3 ~ +15) / VSN_1(-3 ~ - 15) / VSPL_1(+3 ~ +15)

	Mode0	Mode1
VSP	VSP_0(+15)	VSP_1(+3~+15)
VSN	VSN_0(- 15)	VSN_1(-3~- 15)
VSPL	VSPL_0(+3~+15)	VSPL_1(+3~+15)

- If gate voltage is set to +/- 15v, +/- 10v, IC will auto correct source voltage as follows

- VGP- VSP_0 / VSPL_0 / VSP_1 / VSPL_1 >= 2v
- VGN- VSN_0 / VSN_1 >= -2v

For example:

	symbol	Voltage setting	Real Voltage
Voltage	VGP	10v	+10v
	VGN	10v	- 10v
	VSP_0	+15v	+8v
	VSN_0	- 15v	-8v
	VSP_1	+5v	+5v
	VSN_1	-5v	-5v
	VSPL	+15v	+8v



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			VCOM H	+15v+(- 2v)	+8v +(-2v)
			VCOM L	- 15v+(- 2v)	-8v +(-2v)= - 8 v
			VCOMD C	-2v	-2v
Restriction					

8.2.3R02H (POF): Power OFF Command

R02H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
POF	W	0	0	0	0	0	0	0	1	0	02H
1 st Parameter	W	0	-	-	-	-	-	-	-	EDSE	00

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command defines as :										
	<ul style="list-style-type: none"> After power off command, driver will power off base on power off sequence. After power off command, BUSY_N signal will drop from high to low. When finish the power off sequence, BUSY_N signal will rise from low to high . Power off command will turn off charge pump, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating. 										
	1 st parameter										
	Bit	Name	Description								
	0	EDSE	EPD Discharge Trigger 0 : Disable EPD discharge (default) 1 : Enable EPD discharge								
Restriction	This command only active when BUSY_N = “1” .										

8.2.4 R03H (PFS): Power off Sequence Setting Register



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R03H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PFS	W	0	0	0	0	0	0	0	1	1	03H
1 st Parameter	W	1	-	-	T_VDPG_OFF [1:0]	-	-	-	T_VDS_OFF [1:0]	-	00h
2 nd Parameter	W	1	-	-	VGP_LEN[3:0]	-	-	VGP_EXT[3:0]	-	-	54h
3 rd Parameter	W	1	-	-	XON_DLY[3:0]	-	-	XON_LEN[3:0]	-	-	44h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	-The command defines as :		
	1 st Parameter:		
	Bit	Name	Description
	1-0	T_VDS_OFF	Power off sequence of VSP /VSN 00: 20 ms (default) 01: 40 ms 10: 60 ms 11: 80 ms
	5-4	T_VDPG_OFF	Power off sequence of VGP and VGN 00: 20 ms (default) 01: 40 ms 10: 60 ms 11: 80 ms
	2 nd Parameter		
Bit	Name	Description	
1-0	VGP_EXT	VGP extension time 0000: 0 ms 0001: 500 ms 0010: 1000 ms 0011: 1500 ms 0100: 2000 ms (default) 0101: 2500 ms 0110: 3000 ms 0111: 3500 ms 1000: 4000 ms 1001: 4500 ms 1010: 5000 ms 1011: 5500 ms 1100: 6000 ms 1101: 6500 ms	



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	7-4	VGP_LEN	<p>When power off, the length of time VGP stay 10V</p> <p>0000: 0 ms 0001: 500 ms 0010: 1000 ms 0011: 1500 ms 0100: 2000 ms 0101: 2500 ms (default) 0110: 3000 ms 0111: 3500 ms 1000: 4000 ms 1001: 4500 ms 1010: 5000 ms 1011: 5500 ms</p>
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8.2.5 R04H (PON): Power ON Command

R04H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PON	W	0	0	0	0	0	0	1	0	0	04H

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	<p>-The command defines as :</p> <ul style="list-style-type: none"> After power on command, driver will power on base on power on sequence. After power on command, BUSY_N signal will drop from high to low. When finishing the power on sequence(base on PWR command), BUSY_N signal will rise from low to high.
Restriction	This command only active when BUSY_N = “1” .

8.2.6 R06H (BTST): Booster Soft Start Command

R06H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
BTST	W	0	0	0	0	0	0	1	1	0	06H
1 st Parameter	W	1	-	-	-	-	PHB_SFT [1:0]		PHA_SFT [1:0]		00h
2 nd Parameter	W	1	-	-	PHA_ON [5:0]						02h
3 rd Parameter	W	1	-	-	PHA_OFF [5:0]						07h
4 th Parameter	W	1	-	-	PHB_ON [5:0]						02h
5 th Parameter	W	1	-	-	PHB_OFF [5:0]						07h
6 th Parameter	W	1	-	-	PHC_ON [5:0]						02h
7 th Parameter	W	1	-	-	PHC_OFF [5:0]						07h



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Description	-The command define as follows: 1st Parameter:						
	Bit	Name	Description				
	1-0	PHA_SFT	Soft start period of phase A: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS				
	3-2	PHB_SFT	Soft start period of phase B: 00: 10mS (default) 01: 20mS 10: 30mS 11: 40mS				
		Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
		000000	strength1	010110	strength23	101100	strength45
		000001	strength2	010111	strength24	101101	strength46
		000010	strength3	011000	strength25	101110	strength47
		000011	strength4	011001	strength26	101111	strength48
		000100	strength5	011010	strength27	110000	strength49
		000101	strength6	011011	strength28	110001	strength50
		000110	strength7	011100	strength29	110010	strength51
		000111	strength8	011101	strength30	110011	strength52
		001000	strength9	011110	strength31	110100	strength53
		001001	strength10	011111	strength32	110101	strength54
		001010	strength11	100000	strength33	110110	strength55
		001011	strength12	100001	strength34	110111	strength56
		001100	strength13	100010	strength35	111000	strength57
		001101	strength14	100011	strength36	111001	strength58
	001110	strength15	100100	strength37	111010	strength59	
	001111	strength16	100101	strength38	111011	strength60	
	010000	strength17	100110	strength39	111100	strength61	
	010001	strength18	100111	strength40	111101	strength62	
	010010	strength19	101000	strength41	111110	strength63	



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	010011	strength20	101001	strength42	111111	strength64
	010100	strength21	101010	strength43		
	010101	strength22	101011	strength44		

Description	Bit[5:0]	Description	Bit[5:0]	Description	Bit[5:0]	Description
Minimum OFF time setting of PHA_OFF & PHB_OFF & PHC_OFF	000000	Period1	010110	Period23	101100	Period45
	000001	Period2	010111	Period24	101101	Period46
	000010	Period3	011000	Period25	101110	Period47
	000011	Period4	011001	Period26	101111	Period48
	000100	Period5	011010	Period27	110000	Period49
	000101	Period6	011011	Period28	110001	Period50
	000110	Period7	011100	Period29	110010	Period51
	000111	Period8	011101	Period30	110011	Period52
	001000	Period9	011110	Period31	110100	Period53
	001001	Period10	011111	Period32	110101	Period54
	001010	Period11	100000	Period33	110110	Period55
	001011	Period12	100001	Period34	110111	Period56
	001100	Period13	100010	Period35	111000	Period57
	001101	Period14	100011	Period36	111001	Period58
	001110	Period15	100100	Period37	111010	Period59
	001111	Period16	100101	Period38	111011	Period60
	010000	Period17	100110	Period39	111100	Period61
	010001	Period18	100111	Period40	111101	Period62
	010010	Period19	101000	Period41	111110	Period63
	010011	Period20	101001	Period42	111111	Period64
	010100	Period21	101010	Period43		
	010101	Period22	101011	Period44		
Restriction						



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8.2.7 R07H (DSLTP): Deep Sleep Command

R07H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DSLTP	W	0	0	0	0	0	0	1	1	1	07H
1 st Parameter	W	1	1	0	1	0	0	1	0	1	A5h

NOTE: “-” Don’t care, can be set to VDD or GND level

Description	<p>The command define as follows:</p> <p>After this command is transmitted, the chip would enter the deep-sleep mode to save power. The deep sleep mode would return to standby by hardware reset.</p> <p>The only one parameter is a check code, the command would be excited if check code = 0xA5.</p>
Restriction	This command only active when BUSY_N = “1” .

8.2.8 R10H (DTM): Data Start transmission Register

R10H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DTM	W	0	0	0	0	1	0	0	0	0	10H
2 bit mode	W	1									
1 st Parameter	W	1	Pixel1		Pixel2		Pixel3		Pixel4		00h
:			:		:		:		:		00h
:	W	1	:		:		:		:		00h
M th Parameter	W	1	Pixel(n-3)		Pixel(n-2)		Pixel(n-1)		Pixel(n)		00h

Description

The command define as follows:
The register is indicates that user start to transmit data, then write to SRAM. While data transmission complete, user must send command 12H. Then chip will start to send data/VCOM for panel.

Pixel [1~n][1:0]: 2-bit/pixel

Image Data	DDX=1(default)		DDX=0	
Pixel[1:0]	Gray level select	IP output LUT select	Gray level select	IP output LUT select
00b	Gray0	ogray00	Gray3	ogray03
01b	Gray1	ogray01	Gray2	ogray02
10b	Gray2	ogray02	Gray1	ogray01



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	11b	Gray3	ogray03	Gray0	ogray00
	<p>Data mapping example:</p> <p>When DDX=1, Pixel[1:0]=01 -> Gray level select=Gray1, follow LUT data output from IP output port "ogray01".</p> <p>When DDX=0, Pixel[1:0]=11 -> Gray level select=Gray0, follow LUT data output from IP output port "ogray00".</p>				
Restriction					

8.2.9 R11H (DSP): Data Stop Command

R11H	Bit																
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code						
DSP	W	0	0	0	0	1	0	0	0	1	11H						
1 st Parameter	R	1	Data_flag	-	-	-	-	-	-	-	-						
Description	<p>The command defines as :</p> <ul style="list-style-type: none"> While finished the data transmitting, user must send this command to driver and read Data_flag information. <p>1st Parameter:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>7</td> <td>Data_flag</td> <td>0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data.</td> </tr> </tbody> </table> <p>After "Data Start" (10h) or "Data Stop" (11h) commands and when data_flag=1, BUSY_N signal will become "0" and the refreshing of panel starts .</p>											Bit	Name	Description	7	Data_flag	0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data.
Bit	Name	Description															
7	Data_flag	0: Driver didn't receive all the data. 1: Driver has already received all of the one frame data.															
Restriction	This command only actives when BUSY_N = "1" .																

8.2.10 R12H (DRF): Display Refresh Command

R12H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
DRF	W	0	0	0	0	1	0	0	1	0	12H
1 st Parameter	W	1	-	-	-	-	-	Gate_seq	-	AC/D C VCO M	00h



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Description	<p>-The command defines as :</p> <p>While users send this command, driver will refresh display (data/VCOM) base on SRAM data and LUT.</p> <p>AC/DC VCOM:</p> <p>0: AC VCOM, VCOM will follow LUTC when updating image. (default)</p> <p>1: DC VCOM, VCOM will always be VCOMDC when updating image</p> <p>After display refresh command, BUSY_N signal will become "0"</p>
Restriction	This command only actives when BUSY_N = "1"

8.2.11 R17H (AUTO): Auto Sequence

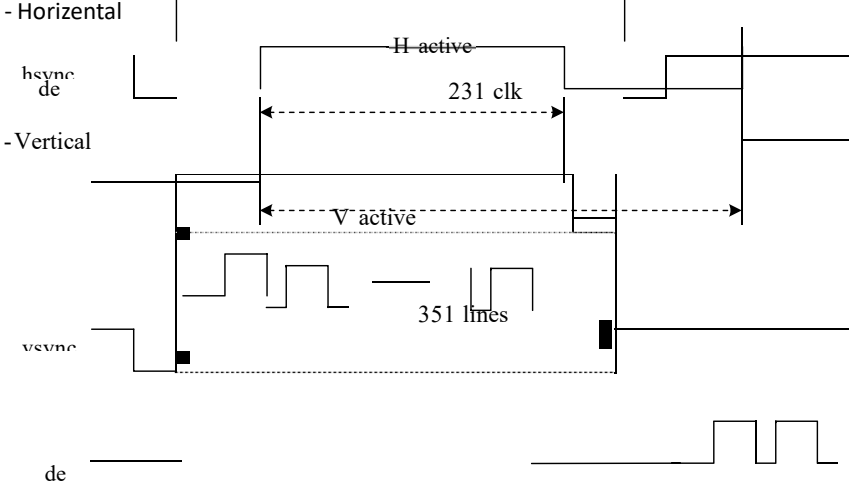
R17H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
Auto Sequence	W	0	0	0	0	1	0	1	1	1	17H
1 st Parameter	W	1	Code[7]	Code[6]	Code[5]	Code[4]	Code[3]	Code[2]	Code[1]	Code[0]	A5h
Description	<p>The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to avoid unnecessary power consumption and reduce the complexity of host's control procedure. The sequence contains several operations, including PON, DRF, POF, DSLP.</p> <p>AUTO (0x17) + Code(0xA5) = (PON→ DRF→ POF)</p> <p>AUTO (0x17) + Code(0xA7) = (PON→ DRF→ POF→ DSLP)</p>										
Restriction	This command only actives when BUSY_N = "1"										

8.2.12 R30H (PLL): PLL Control Register

R30H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PLL	W	0	0	0	1	1	0	0	0	0	30H
1 st Parameter	W	1	-	-	-	-	Dyna	FR[2]	FR[1]	FR[0]	02h



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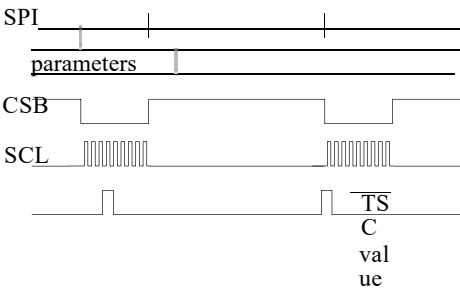
Description	<p>-The command defines as:</p> <p>The command controls the PLL clock frequency. The PLL structure must support the following frame rates:</p> <table border="1" data-bbox="683 459 1093 593"> <tr> <td>bit3</td> <td>Dynamic frame rate</td> </tr> <tr> <td>0</td> <td>Disable(default)</td> </tr> <tr> <td>1</td> <td>Enable</td> </tr> </table> <table border="1" data-bbox="683 616 1093 996"> <tr> <td>FR[2:0]</td> <td>Frame rate</td> </tr> <tr> <td>000</td> <td>12.5 Hz</td> </tr> <tr> <td>001</td> <td>25 Hz</td> </tr> <tr> <td>010</td> <td>50 Hz(default)</td> </tr> <tr> <td>011</td> <td>65 Hz</td> </tr> <tr> <td>100</td> <td>75 Hz</td> </tr> <tr> <td>101</td> <td>85 Hz</td> </tr> <tr> <td>110</td> <td>100 Hz</td> </tr> <tr> <td>111</td> <td>120 Hz</td> </tr> </table>	bit3	Dynamic frame rate	0	Disable(default)	1	Enable	FR[2:0]	Frame rate	000	12.5 Hz	001	25 Hz	010	50 Hz(default)	011	65 Hz	100	75 Hz	101	85 Hz	110	100 Hz	111	120 Hz
bit3	Dynamic frame rate																								
0	Disable(default)																								
1	Enable																								
FR[2:0]	Frame rate																								
000	12.5 Hz																								
001	25 Hz																								
010	50 Hz(default)																								
011	65 Hz																								
100	75 Hz																								
101	85 Hz																								
110	100 Hz																								
111	120 Hz																								
remark	<p>- Horizontal</p>  <p>- Vertical</p>																								
Restriction																									

8.2.13 R40H (TSC): Temperature Sensor Command

R40H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSC	W	0	0	1	0	0	0	0	0	0	40H
1 st Parameter	R	1	D10/TS[D9/TS[6	D8/TS[5	D7/TS[4	D6/TS[D5/TS[2	D4/TS[1	D3/TS[0	-
2 nd Parameter	R	1	D2/	D1/	D0						-



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Description	<p>-The command define as follows: This command indicates the temperature value. If R41H(TSE) bit7 set to 0, this command reads internal temperature sensor value. If R41H(TSE) bit7 set to 1, this command reads external (LM75) temperature sensor value</p> <p>SPI  command parameters</p> <p>BUSY_N</p> <table border="1"> <thead> <tr> <th>TS[7:0]/D[10:3]</th> <th>T (°C)</th> <th>TS[7:0]/D[10:3]</th> <th>T (°C)</th> <th>TS[7:0]/D[10:3]</th> <th>T (°C)</th> </tr> </thead> <tbody> <tr><td>11100111</td><td>-25</td><td>00000000</td><td>0</td><td>00011001</td><td>25</td></tr> <tr><td>11101000</td><td>-24</td><td>00000001</td><td>1</td><td>00011010</td><td>26</td></tr> <tr><td>11101001</td><td>-23</td><td>00000010</td><td>2</td><td>00011011</td><td>27</td></tr> <tr><td>11101010</td><td>-22</td><td>00000011</td><td>3</td><td>00011100</td><td>28</td></tr> <tr><td>11101011</td><td>-21</td><td>00000100</td><td>4</td><td>00011101</td><td>29</td></tr> <tr><td>11101100</td><td>-20</td><td>00000101</td><td>5</td><td>00011110</td><td>30</td></tr> <tr><td>11101101</td><td>-19</td><td>00000110</td><td>6</td><td>00011111</td><td>31</td></tr> <tr><td>11101110</td><td>-18</td><td>00000111</td><td>7</td><td>00100000</td><td>32</td></tr> <tr><td>11101111</td><td>-17</td><td>00001000</td><td>8</td><td>00100001</td><td>33</td></tr> <tr><td>11110000</td><td>-16</td><td>00001001</td><td>9</td><td>00100010</td><td>34</td></tr> <tr><td>11110001</td><td>-15</td><td>00001010</td><td>10</td><td>00100011</td><td>35</td></tr> <tr><td>11110010</td><td>-14</td><td>00001011</td><td>11</td><td>00100100</td><td>36</td></tr> <tr><td>11110011</td><td>-13</td><td>00001100</td><td>12</td><td>00100101</td><td>37</td></tr> <tr><td>11110100</td><td>-12</td><td>00001101</td><td>13</td><td>00100110</td><td>38</td></tr> <tr><td>11110101</td><td>-11</td><td>00001110</td><td>14</td><td>00100111</td><td>39</td></tr> <tr><td>11110110</td><td>-10</td><td>00001111</td><td>15</td><td>00101000</td><td>40</td></tr> <tr><td>11110111</td><td>-9</td><td>00010000</td><td>16</td><td>00101001</td><td>41</td></tr> <tr><td>11111000</td><td>-8</td><td>00010001</td><td>17</td><td>00101010</td><td>42</td></tr> <tr><td>11111001</td><td>-7</td><td>00010010</td><td>18</td><td>00101011</td><td>43</td></tr> <tr><td>11111010</td><td>-6</td><td>00010011</td><td>19</td><td>00101100</td><td>44</td></tr> <tr><td>11111011</td><td>-5</td><td>00010100</td><td>20</td><td>00101101</td><td>45</td></tr> <tr><td>11111100</td><td>-4</td><td>00010101</td><td>21</td><td>00101110</td><td>46</td></tr> <tr><td>11111101</td><td>-3</td><td>00010110</td><td>22</td><td>00101111</td><td>47</td></tr> <tr><td>11111110</td><td>-2</td><td>00010111</td><td>23</td><td>00110000</td><td>48</td></tr> <tr><td>11111111</td><td>-1</td><td>00011000</td><td>24</td><td>00110001</td><td>49</td></tr> </tbody> </table> <p>TS C val ue</p> <table border="1"> <thead> <tr> <th>TS[9:8]</th> <th>T (°C)</th> </tr> </thead> <tbody> <tr><td>00</td><td>+0</td></tr> <tr><td>01</td><td>+0.25</td></tr> <tr><td>10</td><td>+0.5</td></tr> <tr><td>11</td><td>+0.75</td></tr> </tbody> </table>					TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	11100111	-25	00000000	0	00011001	25	11101000	-24	00000001	1	00011010	26	11101001	-23	00000010	2	00011011	27	11101010	-22	00000011	3	00011100	28	11101011	-21	00000100	4	00011101	29	11101100	-20	00000101	5	00011110	30	11101101	-19	00000110	6	00011111	31	11101110	-18	00000111	7	00100000	32	11101111	-17	00001000	8	00100001	33	11110000	-16	00001001	9	00100010	34	11110001	-15	00001010	10	00100011	35	11110010	-14	00001011	11	00100100	36	11110011	-13	00001100	12	00100101	37	11110100	-12	00001101	13	00100110	38	11110101	-11	00001110	14	00100111	39	11110110	-10	00001111	15	00101000	40	11110111	-9	00010000	16	00101001	41	11111000	-8	00010001	17	00101010	42	11111001	-7	00010010	18	00101011	43	11111010	-6	00010011	19	00101100	44	11111011	-5	00010100	20	00101101	45	11111100	-4	00010101	21	00101110	46	11111101	-3	00010110	22	00101111	47	11111110	-2	00010111	23	00110000	48	11111111	-1	00011000	24	00110001	49	TS[9:8]	T (°C)	00	+0	01	+0.25	10	+0.5	11	+0.75
	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)	TS[7:0]/D[10:3]	T (°C)																																																																																																																																																																					
11100111	-25	00000000	0	00011001	25																																																																																																																																																																						
11101000	-24	00000001	1	00011010	26																																																																																																																																																																						
11101001	-23	00000010	2	00011011	27																																																																																																																																																																						
11101010	-22	00000011	3	00011100	28																																																																																																																																																																						
11101011	-21	00000100	4	00011101	29																																																																																																																																																																						
11101100	-20	00000101	5	00011110	30																																																																																																																																																																						
11101101	-19	00000110	6	00011111	31																																																																																																																																																																						
11101110	-18	00000111	7	00100000	32																																																																																																																																																																						
11101111	-17	00001000	8	00100001	33																																																																																																																																																																						
11110000	-16	00001001	9	00100010	34																																																																																																																																																																						
11110001	-15	00001010	10	00100011	35																																																																																																																																																																						
11110010	-14	00001011	11	00100100	36																																																																																																																																																																						
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11111001	-7	00010010	18	00101011	43																																																																																																																																																																						
11111010	-6	00010011	19	00101100	44																																																																																																																																																																						
11111011	-5	00010100	20	00101101	45																																																																																																																																																																						
11111100	-4	00010101	21	00101110	46																																																																																																																																																																						
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11111110	-2	00010111	23	00110000	48																																																																																																																																																																						
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TS[9:8]	T (°C)																																																																																																																																																																										
00	+0																																																																																																																																																																										
01	+0.25																																																																																																																																																																										
10	+0.5																																																																																																																																																																										
11	+0.75																																																																																																																																																																										
Restriction	This command only actives when BUSY_N = "1" .																																																																																																																																																																										



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8.2.14 R41H (TSE): Temperature Sensor Calibration Register

R41H	Bit																						
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code												
TSE	W	0	0	1	0	0	0	0	0	1	41H												
1 st Parameter	W	1	TSE	-	-	TO[4]	TO[3]	TO[2]	TO[1]	TO[0]	00h												
Description	-The command defines as: This command indicates the driver IC temperature sensor enable and calibration function. Reserve one temperature offset TO[3:0] for calibration 1. TO[3]: mean '+' or '-', while 0 is '+' ; 1 is '-' 2. TO[2:0]: mean temperature offset value																						
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>3-0</td> <td>TO[3:0]</td> <td> Temperature level: 0000: +0°C (default) 0001: +0.5°C 0010: +1°C 0011: +1.5°C 0100: +2°C 0101: +2.5°C 0110: +3°C 0111: +3.5°C 1000: -4°C 1001: -3.5°C 1010: -3°C 1011: -2.5°C 1100: -2°C 1101: -1.5°C 1110: -1°C 1111: -0.5°C </td> </tr> <tr> <td>4</td> <td>TO[4]</td> <td> 0: +0.0°C (default) 1: +0.25°C </td> </tr> <tr> <td>7</td> <td>TSE</td> <td> Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor. </td> </tr> </tbody> </table>											Bit	Name	Description	3-0	TO[3:0]	Temperature level: 0000: +0°C (default) 0001: +0.5°C 0010: +1°C 0011: +1.5°C 0100: +2°C 0101: +2.5°C 0110: +3°C 0111: +3.5°C 1000: -4°C 1001: -3.5°C 1010: -3°C 1011: -2.5°C 1100: -2°C 1101: -1.5°C 1110: -1°C 1111: -0.5°C	4	TO[4]	0: +0.0°C (default) 1: +0.25°C	7	TSE	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.
	Bit	Name	Description																				
	3-0	TO[3:0]	Temperature level: 0000: +0°C (default) 0001: +0.5°C 0010: +1°C 0011: +1.5°C 0100: +2°C 0101: +2.5°C 0110: +3°C 0111: +3.5°C 1000: -4°C 1001: -3.5°C 1010: -3°C 1011: -2.5°C 1100: -2°C 1101: -1.5°C 1110: -1°C 1111: -0.5°C																				
4	TO[4]	0: +0.0°C (default) 1: +0.25°C																					
7	TSE	Internal temperature sensor enable 0: Internal temperature sensor enable.(default) 1: Internal temperature sensor disable, using external temperature sensor.																					
Restriction																							
This command only actives after R04H(PON)																							

8.2.15 R42H (TSW): Temperature Sensor Write Register

R42H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TSW	W	0	0	1	0	0	0	0	1	0	42H
1 st Parameter	W	1	WATTR[7]	WATTR[6]	WATTR[5]	WATTR[4]	WATTR[3]	WATTR[2]	WATTR[1]	WATTR[0]	00h
2 nd Parameter	W	1	WMSB[7]	WMSB[6]	WMSB[5]	WMSB[4]	WMSB[3]	WMSB[2]	WMSB[1]	WMSB[0]	00h
3 rd Parameter	W	1	WLSB[7]	WLSB[6]	WLSB[5]	WLSB[4]	WLSB[3]	WLSB[2]	WLSB[1]	WLSB[0]	00h



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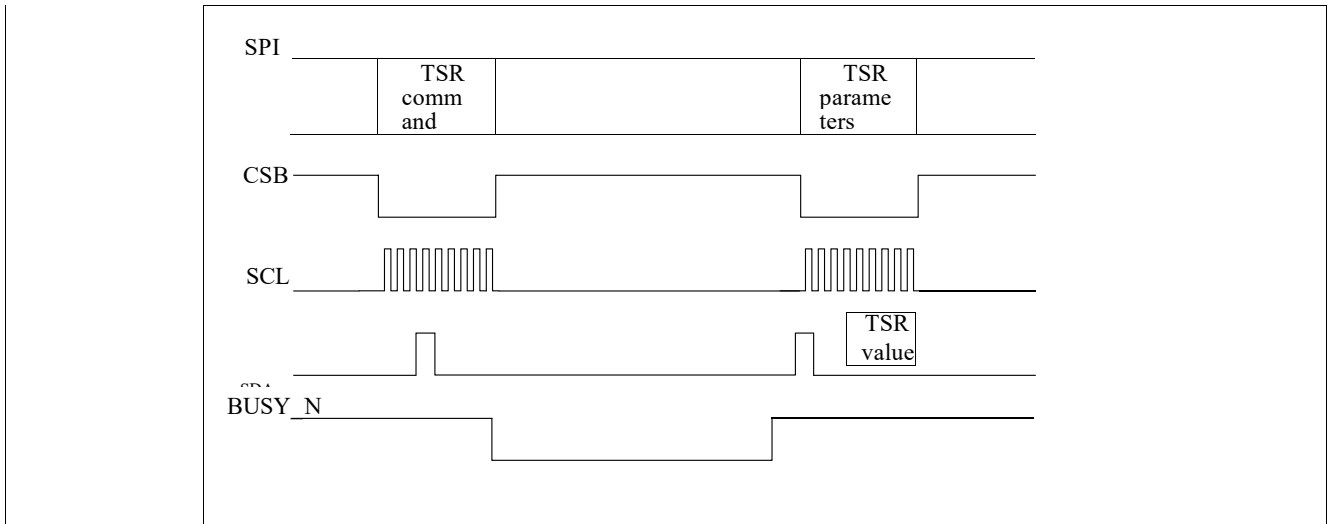
Description	<p>-The command defines as: This command writes the temperature.</p> <p>1st Parameter:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>2-0</td> <td>WATTR[2:0]</td> <td>Pointer setting</td> </tr> <tr> <td>5-3</td> <td>WATTR[5:3]</td> <td>User-defined address bits (A2, A1, A0)</td> </tr> <tr> <td>7-6</td> <td>WATTR[7:6]</td> <td>I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)</td> </tr> </tbody> </table> <p>2nd Parameter:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>7-0</td> <td>WMSB[7:0]</td> <td>MSByte of write-data to external temperature sensor</td> </tr> </tbody> </table> <p>3rd Parameter:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>7-0</td> <td>WLSB[7:0]</td> <td>LSByte of write-data to external temperature sensor</td> </tr> </tbody> </table>											Bit	Name	Description	2-0	WATTR[2:0]	Pointer setting	5-3	WATTR[5:3]	User-defined address bits (A2, A1, A0)	7-6	WATTR[7:6]	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)	Bit	Name	Description	7-0	WMSB[7:0]	MSByte of write-data to external temperature sensor	Bit	Name	Description	7-0	WLSB[7:0]	LSByte of write-data to external temperature sensor
Bit	Name	Description																																	
2-0	WATTR[2:0]	Pointer setting																																	
5-3	WATTR[5:3]	User-defined address bits (A2, A1, A0)																																	
7-6	WATTR[7:6]	I2C Write Byte Number 00: 1 byte (head byte only) 01: 2 bytes (head byte + pointer) 10: 3 bytes (head byte + pointer + 1st parameter) 11: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)																																	
Bit	Name	Description																																	
7-0	WMSB[7:0]	MSByte of write-data to external temperature sensor																																	
Bit	Name	Description																																	
7-0	WLSB[7:0]	LSByte of write-data to external temperature sensor																																	
Restriction	This command only activates after R04H(PON)																																		

8.2.16 R43H (TSR): Temperature Sensor Read Register

R43H	Bit																						
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code												
TSR	W	0	0	1	0	0	0	0	1	1	43H												
1 st Parameter	R	1	RMSB[7]	RMSB[6]	RMSB[5]	RMSB[4]	RMSB[3]	RMSB[2]	RMSB[1]	RMSB[0]	-												
2 nd Parameter	R	1	RLSB[7]	RLSB[6]	RLSB[5]	RLSB[4]	RLSB[3]	RLSB[2]	RLSB[1]	RLSB[0]	-												
Description	<p>-The command defines as: This command reads the temperature sensed by the temperature sensor.</p> <p>1st Parameter:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>7-0</td> <td>RMSB[7:0]</td> <td>MSByte of read-data from external temperature sensor</td> </tr> </tbody> </table> <p>2nd Parameter:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>7-0</td> <td>RLSB[7:0]</td> <td>LSByte of write-data from external temperature sensor</td> </tr> </tbody> </table>											Bit	Name	Description	7-0	RMSB[7:0]	MSByte of read-data from external temperature sensor	Bit	Name	Description	7-0	RLSB[7:0]	LSByte of write-data from external temperature sensor
Bit	Name	Description																					
7-0	RMSB[7:0]	MSByte of read-data from external temperature sensor																					
Bit	Name	Description																					
7-0	RLSB[7:0]	LSByte of write-data from external temperature sensor																					



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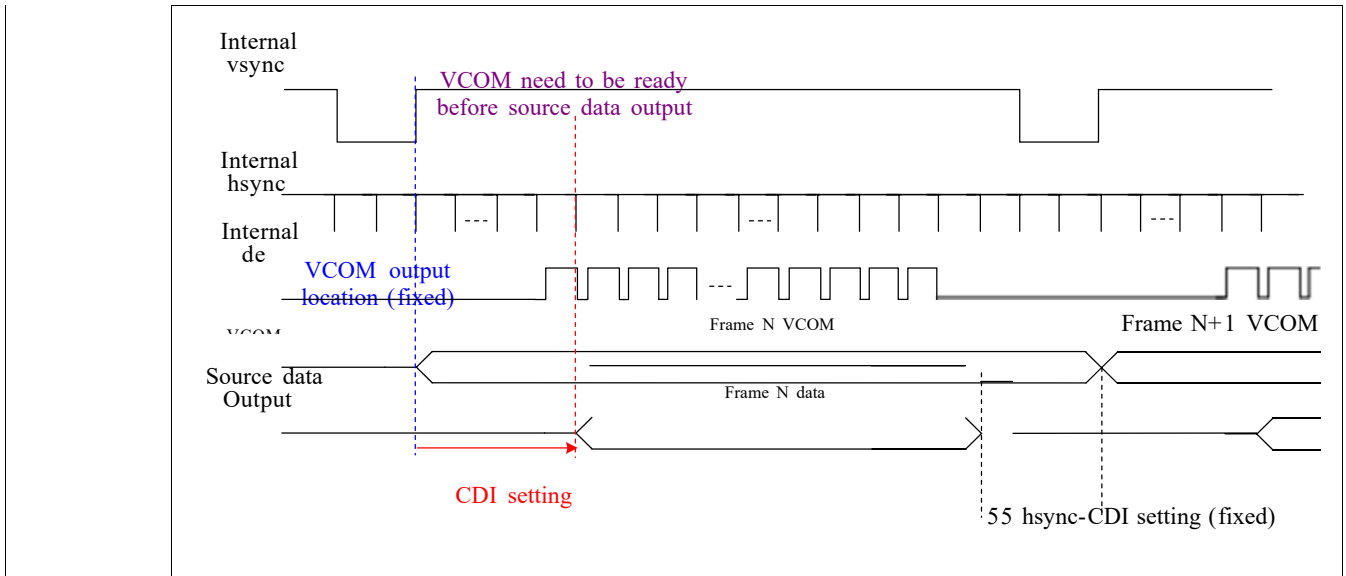
Restriction	This command only actives after R04H(PON)
-------------	-------------------------------------------

8.2.17 R50H (CDI): VCOM and DATA interval setting Register

R50H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
CDI	W	0	0	1	0	1	0	0	0	0	50H
1 st Parameter	W	1	VBD[2]	VBD[1]	VBD[0]	DDX	CDI[3]	CDI[2]	CDI[1]	CDI[0]	97h
Description	-The command defines as: This command can set 2 kinds of parameters, 1.VCOM to data output interval(CDI) : CDI[3:0]: This command indicates the interval of VCOM and data output. When setting the vertical back porch, the total blanking will be keep (55hsync).										
	Bit	Name	Description								
3-0	CDI[3:0]	Vcom and data interval 0000: 17 hsync 0001:16 hsync 0010:15 hsync 0011:14 hsync 0100:13 hsync 0101:12 hsync 0110:11 hsync 0111:10 hsync(default) 1000:9 hsync 1001:8 hsync 1010:7 hsync 1011:6 hsync 1100:5 hsync 1101:4 hsync 1110:3 hsync 1111:2 hsync									



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VBD[2:0]: Border data selection. (from LUT output by IP port border_w[1:0])
 This register will make boarder pin output being mapped to a certain gray scale.

Bit 4	Bit7-5	Description	IP setting for Border LUT select
0	VBD[2:0]	Gray level	
0	000	Floating	N/A
	001	Gray3	border_buf=011
	010	Gray2	border_buf=010
	011	Gray1	border_buf=001
	100	Gray0	border_buf=000
1 (default)	000	Gray0	border_buf=000
	001	Gray1	border_buf=001
	010	Gray2	border_buf=010
	011	Gray3	border_buf=011
	100	Floating	N/A

Border output voltage level: The level selection is based on mapping LUT data.
 Ex: Gray 1 waveform is mapping to 15V, without VCOM offset, the real output on Boarder pin shall be 15V.
 Boarder output will follow FOPT definition being defined in R00h.

Restriction

8.2.18 R51H (LPD): Lower Power Detection Register

R51H	Bit											
	Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LPD	W	0	0	1	0	1	0	0	0	0	1	51H
1 st Parameter	R	1	-	-	-	-	-	-	-	-	LPD	--



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Description	<p>-The command defines as: This command indicates the input power condition. Host can read this data to understand the battery's condition. When LPD="1", system input power is normal. When LPD="0", system input power is lower (VDD<2.5v, which could be select in RE4H (LVSEL)).</p> <p>1st Parameter:</p> <table border="1" style="margin-left: 20px;"> <tr> <td>Bit 0</td> <td>LPD</td> </tr> <tr> <td>0</td> <td>Low power input.</td> </tr> <tr> <td>1</td> <td>Normal status.</td> </tr> </table>	Bit 0	LPD	0	Low power input.	1	Normal status.
Bit 0	LPD						
0	Low power input.						
1	Normal status.						
Restriction	This command only actives when BUSY_N = "1" .						

8.2.19 R61H (TRES): Resolution setting

R61H	Bit											
	Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
TRES		W	0	0	1	1	0	0	0	0	1	61H
1 st Parameter		W	1	-	-	-	-	-	-	HRES(9)	HRES(8)	00h
2 nd Parameter		W	1	HRES(7)	HRES(6)	HRES(5)	HRES(4)	HRES(3)	HRES(2)	0	0	00h
3 th Parameter		W	1	-	-	-	-	-	-	VRES(9)	VRES(8)	00h
4 th Parameter		W	1	VRES(7)	VRES(6)	VRES(5)	VRES(4)	VRES(3)	VRES(2)	VRES(1)	VRES(0)	00h



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Description	<p>- The command define as follows: When using register: Horizontal display resolution(source) = HRES Vertical display resolution(gate) = VRES</p> <p>Note: No matter HRES[9:8],HRES[1:0],VRST[9] value being filled, it's always be 00b.</p> <p>Channel disable calculation: GD : First G active = G0; LAST active GD= first active +VRES[9:0] - 1 SD : First active channel: =S0 ; LAST active SD= first active +HRES[9:2]*4- 1</p> <p>EX :176X296 GD: First G active = G0 LAST active GD= 0+296- 1= 295; (G295) SD : First active channel: =S0 LAST active SD=0+44*4- 1=175; (S175)</p> <p>Note : Only supports source 176.ch for source 160ch. above</p>
Restriction	Horizontal resolution should be 4-multiple.

8.2.20 R65H(GSST): Gate/Source Start Setting Register

R65H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
GSST	W	0	0	1	1	0	0	1	0	1	65H
1 st Parameter	W	1	-	-	-	-	-	-	S_start[9]	S_start[8]	00h
2 nd Parameter	W	1	S_start[7]	S_start[6]	S_start[5]	S_start[4]	S_start[3]	S_start[2]	0	0	00h
3 rd Parameter	W	1	-	-	-	-	-	-	G_start[9]	G_start[8]	00h
4 th Parameter	W	1	G_start[7]	G_start[6]	G_start[6]	G_start[4]	G_start[3]	G_start[2]	G_start[1]	G_start[0]	00h

Description	<p>-The command define as follows:</p> <p>Note: No matter S_start[9:8], S_start [1:0],VRST[9] value being filled, it's always be 00b.</p> <p>1.S_Start [7:0] describe which source output line is the first date line 2.G_Start[8:0] describe which gate line is the first scan line</p>
Restriction	S_Start should be the multiple of 4

8.2.21 R70H (REV): REVISION register

R70H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV	W	0	0	1	1	1	0	0	0	0	70H
1 st Parameter	R	1	0	0	0	0	0	0	1	1	03h



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2 nd Parameter	R	1	0	0	0	0	0	0	1	0	02h
3 rd Parameter	R	1	0	0	0	0	0	0	0	1	01h

Description	The command defines as: 1 st & 2 nd & 3 rd Parameter:										
	Bit		Description								
	7-0		CHIP_REV								
Restriction											

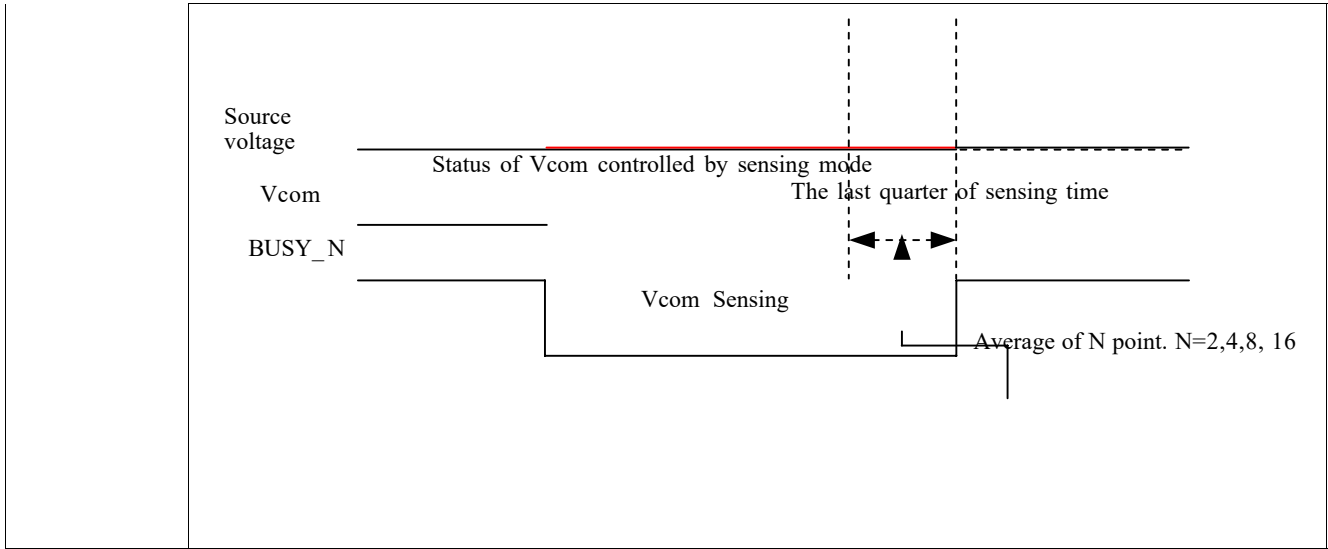
8.2.22 R80H (AMV): Auto Measure VCOM register

R80H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
AMV	W	0	1	0	0	0	0	0	0	0	80H
1 st Parameter	W	1	P[1]	P[0]	AMVT[1]	AMVT[0]	XON	AMVS	AMV	AMVE	00h

Description	- The command defines as: This command indicates the IC status. Host can read this data to understand the IC status.										
	1 st Parameter:										
	Bit		Name		Description						
	0		AMVE		AMVE: Auto Measure Vcom Setting 0: Auto measure VCOM disable (default) 1: Auto measure VCOM enable						
	1		AMV		AMV: Analog signal 0: Get Vcom value from R81h (default) 1: Get Vcom value in analog signal						
	2		AMVS		AMVS: setting for Source output of AMV 0: Source output 0V during Auto Measure VCOM period. (default) 1: Source output VSPL_0 during Auto Measure VCOM period.						
	3		XON		XON: setting for all Gate ON of AMV 0: Gate normally scan during Auto Measure VCOM period. (default) 1: All Gate ON during Auto Measure VCOM period.						
5-4		AMVT[1:0]		The sensing time of VCOM detection 00: 5s (default) 01: 10s 10: 15s 11: 20s							
7-6		P[1:0]		The sensing points of sampling time 00: 2 (default) 01: 4 10: 8 11: 16 Sampling time = the last quarter of sensing time (T) VCOM = average of N points. N=2,4,8,16							



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Restriction This command only actives when BUSY_N = "1" .

8.2.23 R81H (VV): VCOM Value register

R81H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
VV	W	0	1	0	0	0	0	0	0	1	81H
1 st Parameter	R	1	-	VV[6]	VV[5]	VV[4]	VV[3]	VV[2]	VV[1]	VV[0]	--

Description -The command defines as:
This command could get the VCOM value
1st Parameter:

Bit	Name	Description							
VCOM value									
	VCOM[6:0]	Voltage(V)	VCOM[6:0]	Voltage(V)	VCOM[6:0]	Voltage(V)	VCOM[6:0]	Voltage(V)	VCOM[6:0]
6-0	VV[6:0]	00h	0	0011100	1Ch	-1.4	0111000	38h	-2.8
		01h	-0.05	0011101	1Dh	-1.45	0111001	39h	-2.85
		02h	-0.1	0011110	1Eh	-1.5	0111010	3Ah	-2.9
		03h	-0.15	0011111	1Fh	-1.55	0111011	3Bh	-2.95
		04h	-0.2	0100000	20h	-1.6	0111100	3Ch	-3
		05h	-0.25	0100001	21h	-1.65	0111101	3Dh	-3.05
		06h	-0.3	0100010	22h	-1.7	0111110	3Eh	-3.1
		07h	-0.35	0100011	23h	-1.75	0111111	3Fh	-3.15
		08h	-0.4	0100100	24h	-1.8	1000000	40h	-3.2
		09h	-0.45	0100101	25h	-1.85	1000001	41h	-3.25
		0Ah	-0.5	0100110	26h	-1.9	1000010	42h	-3.3
		0Bh	-0.55	0100111	27h	-1.95	1000011	43h	-3.35
		0Ch	-0.6	0101000	28h	-2	1000100	44h	-3.4



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				0001101	0Dh	-0.65	0101001	29h	-2.05	1000101	45h	-3.45
				0001110	0Eh	-0.7	0101010	2Ah	-2.1	1000110	46h	-3.5
				0001111	0Fh	-0.75	0101011	2Bh	-2.15	1000111	47h	-3.55
				0010000	10h	-0.8	0101100	2Ch	-2.2	1001000	48h	-3.6
				0010001	11h	-0.85	0101101	2Dh	-2.25	1001001	49h	-3.65
				0010010	12h	-0.9	0101110	2Eh	-2.3	1001010	4Ah	-3.7
				0010011	13h	-0.95	0101111	2Fh	-2.35	1001011	4Bh	-3.75
				0010100	14h	-1	0110000	30h	-2.4	1001100	4Ch	-3.8
				0010101	15h	-1.05	0110001	31h	-2.45	1001101	4Dh	-3.85
				0010110	16h	-1.1	0110010	32h	-2.5	1001110	4Eh	-3.9
				0010111	17h	-1.15	0110011	33h	-2.55	1001111	4Fh	-3.95
				0011000	18h	-1.2	0110100	34h	-2.6	1010000	50h	-4
				0011001	19h	-1.25	0110101	35h	-2.65	other		-4
				0011010	1Ah	-1.3	0110110	36h	-2.7			
				0011011	1Bh	-1.35	0110111	37h	-2.75			
Restriction												

8.2.24 R82H (VDCS): VCOM_DC Setting Register

R82H	Bit											
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code	
VDCS	W	0	1	0	0	0	0	0	1	0	82H	
1 st Parameter	W	1	MTP V CM	VDCS[6]	VDCS[5]	VDCS [4]	VDCS [3]	VDCS [2]	VDCS [1]	VDCS [0]	00h	
Description	- The command defines as: This command set the VCOM DC value. Driver will base on this value for VCM_DC. 1 st Parameter:											
	Bit	Name	Description									



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VCOM [6:0] Voltage(V)	VCOM[6:0] Voltage(V)	VCOM[6:0] Voltage(V)	VCOM[6:0] Voltage(V)
00000000 00h 0(default)	0011100 1Ch -1.4	0111000 38h -2.8	
00000001 01h -0.05	0011101 1Dh -1.45	0111001 39h -2.85	
00000010 02h -0.1	0011110 1Eh -1.5	0111010 3Ah -2.9	
00000011 03h -0.15	0011111 1Fh -1.55	0111011 3Bh -2.95	
0000100 04h -0.2	0100000 20h -1.6	0111100 3Ch -3	
0000101 05h -0.25	0100001 21h -1.65	0111101 3Dh -3.05	
0000110 06h -0.3	0100010 22h -1.7	0111110 3Eh -3.1	
0000111 07h -0.35	0100011 23h -1.75	0111111 3Fh -3.15	
0001000 08h -0.4	0100100 24h -1.8	1000000 40h -3.2	
0001001 09h -0.45	0100101 25h -1.85	1000001 41h -3.25	
0001010 0Ah -0.5	0100110 26h -1.9	1000010 42h -3.3	
0001011 0Bh -0.55	0100111 27h -1.95	1000011 43h -3.35	
0001100 0Ch -0.6	0101000 28h -2	1000100 44h -3.4	
0001101 0Dh -0.65	0101001 29h -2.05	1000101 45h -3.45	
0001110 0Eh -0.7	0101010 2Ah -2.1	1000110 46h -3.5	
0001111 0Fh -0.75	0101011 2Bh -2.15	1000111 47h -3.55	
0010000 10h -0.8	0101100 2Ch -2.2	1001000 48h -3.6	
0010001 11h -0.85	0101101 2Dh -2.25	1001001 49h -3.65	
0010010 12h -0.9	0101110 2Eh -2.3	1001010 4Ah -3.7	
0010011 13h -0.95	0101111 2Fh -2.35	1001011 4Bh -3.75	
0010100 14h -1	0110000 30h -2.4	1001100 4Ch -3.8	
0010101 15h -1.05	0110001 31h -2.45	1001101 4Dh -3.85	
0010110 16h -1.1	0110010 32h -2.5	1001110 4Eh -3.9	
0010111 17h -1.15	0110011 33h -2.55	1001111 4Fh -3.95	
0011000 18h -1.2	0110100 34h -2.6	1010000 50h -4	
0011001 19h -1.25	0110101 35h -2.65	other -4	
0011010 1Ah -1.3	0110110 36h -2.7		
0011011 1Bh -1.35	0110111 37h -2.75		



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	7	MTP_VCM	Follow MTP VCOM value in MTP mode 0: From the setting of MTP (default) 1: From the setting of register
Restriction			

8.2.25 R83H (PTL): Partial Window Register

R83H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PTL	W	0	1	0	0	0	0	0	1	1	83H
1 st Parameter	W	1	-	-	-	-	-	-	HRST[9]	HRST[8]	00h
2 nd Parameter	W	1	HRST[7]	HRST[6]	HRST[5]	HRST[4]	HRST[3]	HRST[2]	-	-	00h
3 rd Parameter	W	1	-	-	-	-	-	-	HRED[9]	HRED[8]	00h
4 th Parameter	W	1	HRED[7]	HRED[6]	HRED[5]	HRED[4]	HRED[3]	HRED[2]	-	-	00h
5 th Parameter	W	1	-	-	-	-	-	-	VRST[9]	VRST[8]	00h
6 th Parameter	W	1	VRST[7]	VRST[6]	VRST[5]	VRST[4]	VRST[3]	VRST[2]	VRST[1]	VRST[0]	00h
7 th Parameter	W	1	-	-	-	-	-	-	VRED[9]	VRED[8]	00h
8 th Parameter	W	1	VRED[7]	VRED[6]	VRED[5]	VRED[4]	VRED[3]	VRED[2]	VRED[1]	VRED[0]	00h
9 th Parameter	W	1	-	-	-	-	-	-	-	PMODE	00h
Description	_This command sets partial window.										
	Name		Description								
	HRST[9:2]		Horizontal start address								
	HRED[9:2]		Horizontal end address. HRED must be greater than HRST.								
	VRST[9:0]		Vertical start address.								
	VRED[9:0]		Vertical end address. VRED must be greater than VRST.								
	PMODE		0: disable partial mode(default) 1: enable partial mode								
<p>Note: No matter HRST[1:0], HRST[9:8], HRED[9:8], VRST[9], VRED[9] value being filled, it's always be 00b. No matter HRED[1:0] value being filled, it's always be 11b.</p> <p>Gates scan both inside and outside of the partial window.</p>											
Restriction											



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8.2.26 R90H (PGM): Program Mode

R90H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PGM	W	0	1	0	0	1	0	0	0	0	90H
Description	-The command define as follows: After this command is issued, the chip would enter the program mode. The mode would return to standby by hardware reset.										
Restriction											

8.2.27 R91H (APG): Active Program

R91H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
APG	W	0	1	0	0	1	0	0	0	1	91H
Description	-The command define as follows: After this command is transmitted, the programming state machine would be activated.										
Restriction	The BUSY flag would change state from 0 to 1 while the programming is completed										

8.2.28 R92H (RMTP): Read MTP Data

R92H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMTP	W	0	1	0	0	1	0	0	1	0	92H
1 st Parameter	R	1	Dummy								-
2 nd Parameter	R	1	The data of address 0x000 in the MTP								-
3 rd Parameter	R	1	The data of address 0x001 in the MTP								-
4 th Parameter	R	1	:								-
5 th Parameter	R	1	The data of address (n-1) in the MTP								-
6 th ~(m-1) th Parameter	R	1								-
m th Parameter	R	1	The data of address (n) in the MTP								-
Description	-The command define as follows: The command is used for reading the content of MTP for checking the data of programming. The value of (n) is depending on the amount of programmed data, the max address = 0x17FF										

8.2.34 R9EH(REV2): REVISION2 register



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8.2.29 R9EH(REV2): REVISION2 register

R9EH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
REV2	W	0	1	0	0	1	1	1	1	0	9EH
1 st Parameter	R	1	0	0	0	0	0	0	0	1	01h
Description	- The command defines as:										
	1 st Parameter:										
	Bit		Description								
	7-0		CHIP_REV								
Restriction											

8.2.30 R9FH(RMRB) Read MTP Reserved Bytes

R9FH	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
RMRB	W	0	1	0	0	1	1	1	1	1	9FH
1 st Parameter	R	1	Dummy								00h
2 nd Parameter	R	1	The data of address 0x16F7 in the MTP								00h
3 rd Parameter	R	1	:								00h
:	R	1	:								00h
97 th Parameter	R	1	:								00h
98 th Parameter	R	1	:								00h
101 th Parameter	R	1	The data of address 0x175A in the MTP								00h
Description	- The command define as follows:										
	The command is used for reading the content of MTP Reserved Byte for checking the data of programming. This command could read these information from MTP directly.										
Restriction											

8.2.31 RE3H (PWS): Power Saving Register

RE3H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
PWS	W	0	1	1	1	0	0	0	1	1	E3H
1 st Parameter	W	1	VCOM_W[3:0]				SD_W[3:0]				00h



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Description	<p>- This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.</p> <p>VCOM_W: VCOM power saving width (unit = line period)</p> <p>SD_W: Source power saving width (unit = 500nS), SD_W<=S2G</p>
Restriction	

8.2.32 RE4H (LVSEL): LVD Voltage Select Register

RE4H	Bit										
Inst/Para	R/W	D/CX	D7	D6	D5	D4	D3	D2	D1	D0	Code
LVSEL	W	0	1	1	1	0	0	1	0	0	E4H
1 st Parameter	W	1	-	-	-	-	-	-	LVD_SEL[1:0]		03h
Description	LVD_SEL[1:0]: Low Power Voltage Selection										
	LVD_SEL[1:0]			LVD value							
	00			< 2.2 V							
	01			< 2.3 V							
	10			< 2.4 V							
11			< 2.5 V (default)								
Restriction											



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9. FUNCTION DESCRIPTION

9.1 Power On/Off and DSLP Sequence

Power on Sequence

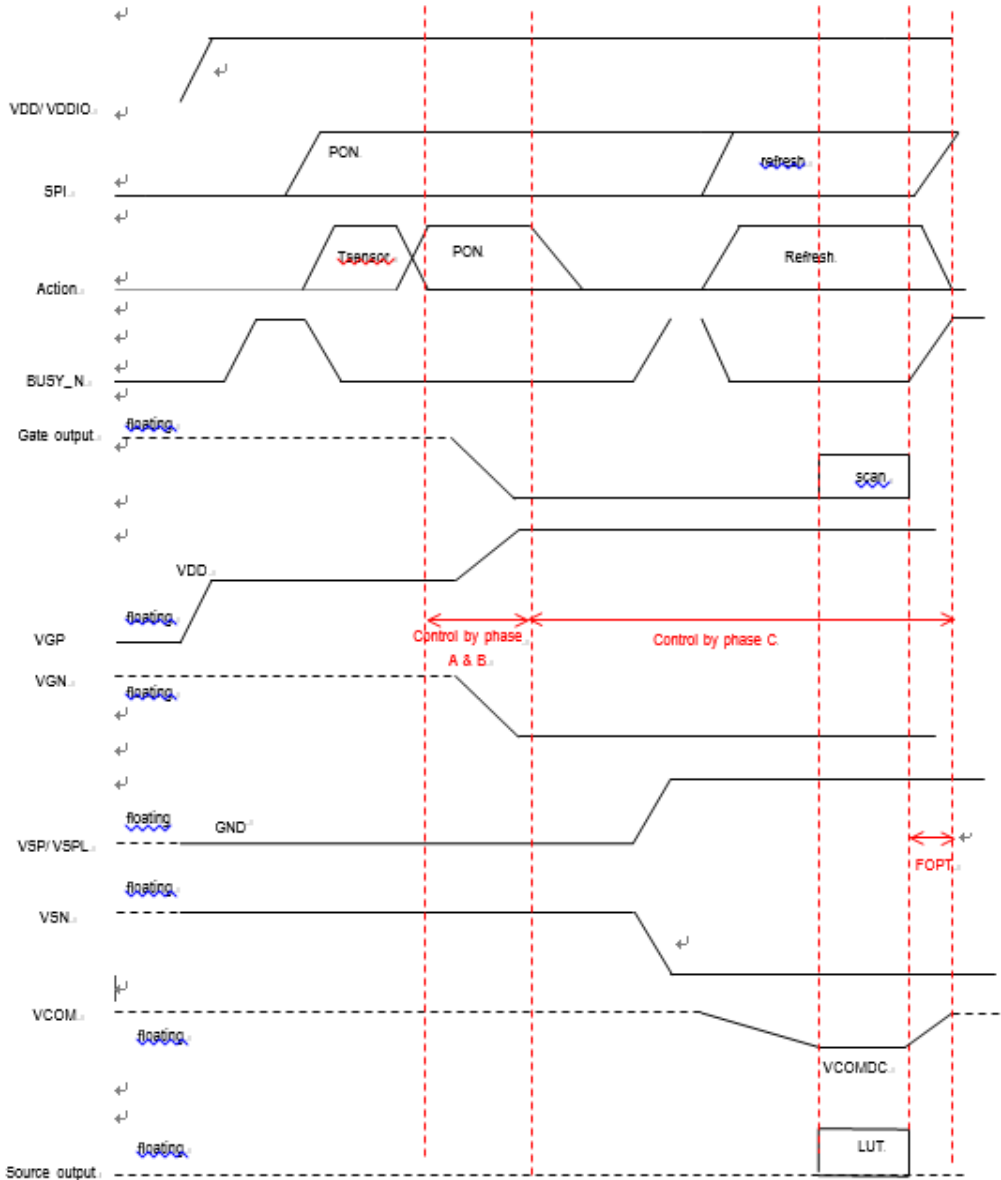


Figure 1: Power on sequence.



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Power off Sequence

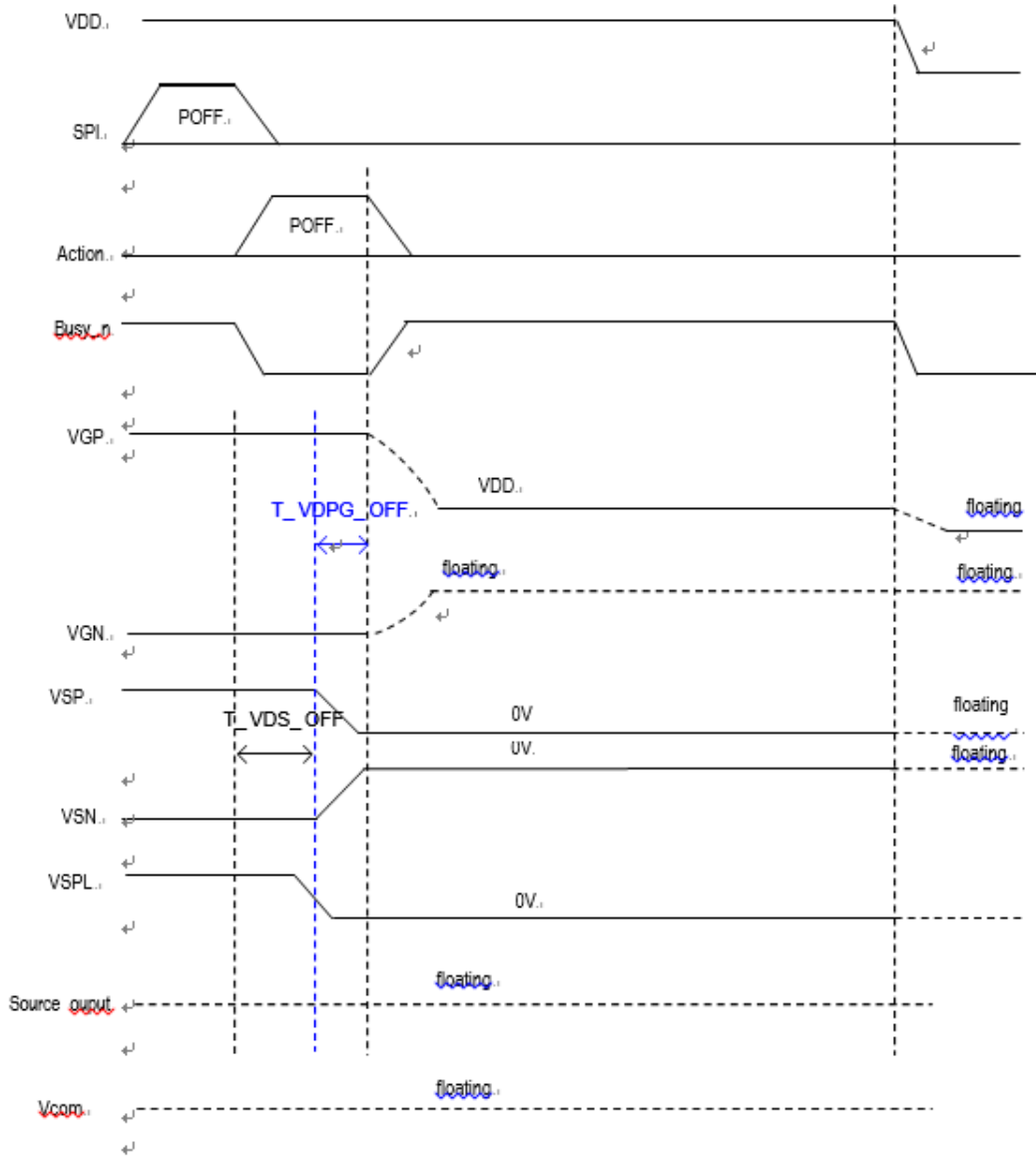


Figure 2: Power off sequence



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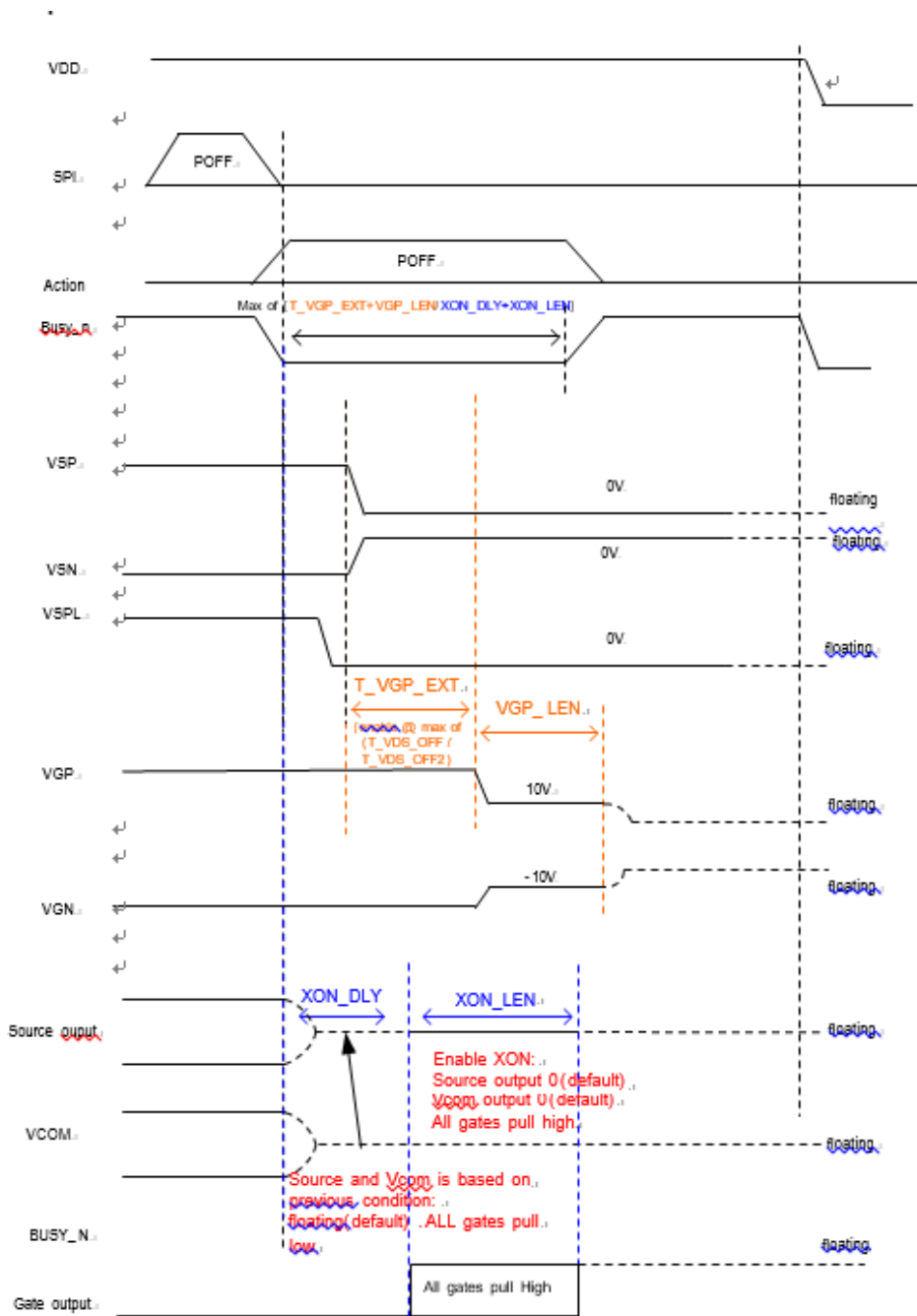


Figure 3: Power off sequence with EPD discharge.



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DSLP sequence.

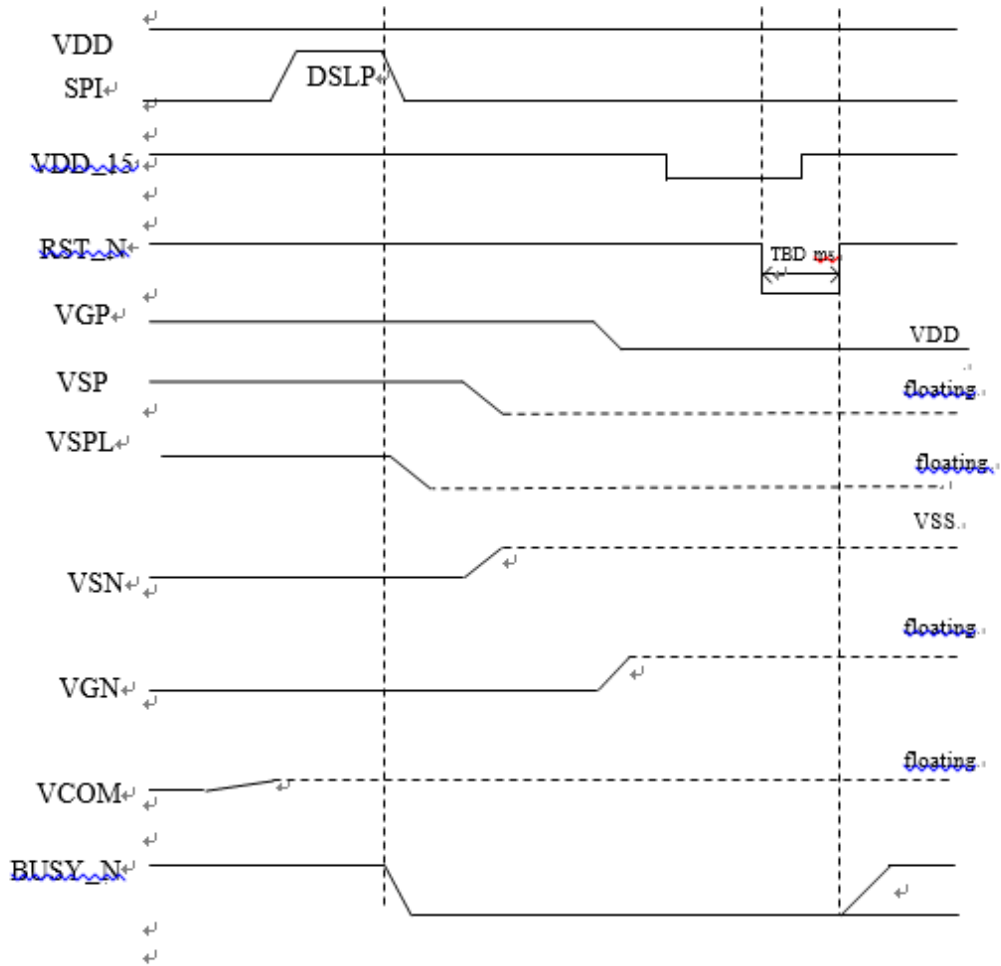


Figure 4: DSLP sequence.



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10. Reference Circuit

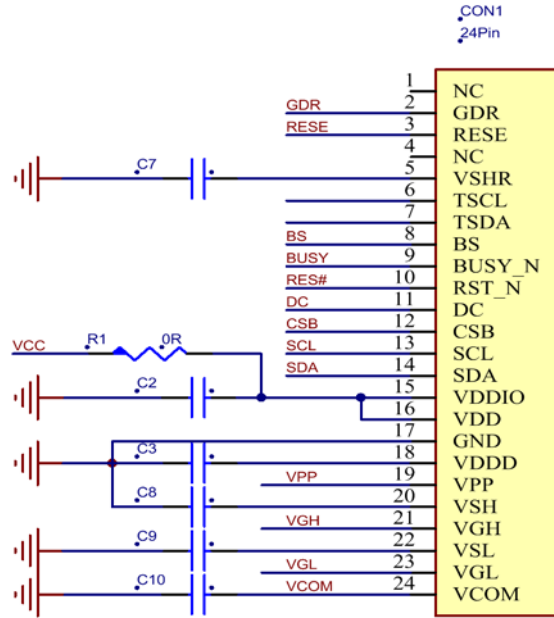


Figure. 9-1

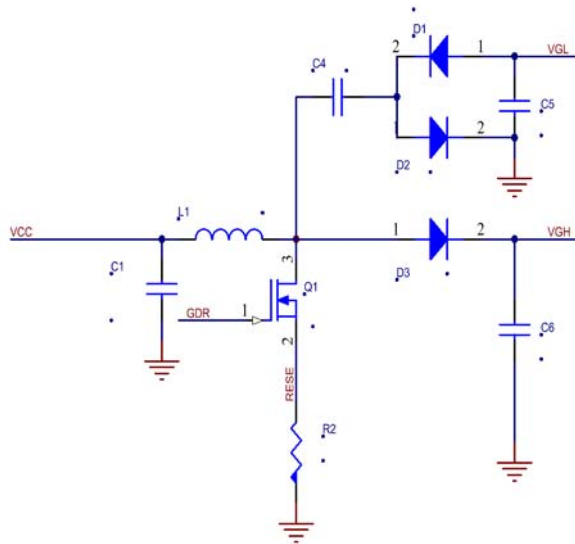


Figure. 9-2



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Part Name	Value /requirement/Reference Part
C1—C3	1uF/0603;X5R;Voltage Rating: 25V
C4-C9	1uF/0603;X5R;Voltage Rating: 50V
C10	0.47uF/0603; X5R;Voltage Rating: 25V
D1—D3	MBR0530 1) Reverse DC voltage \geq 30V 2) Forward current \geq 500mA 3)Forward voltage \leq 430mV
R2	2.2 Ω /0603; 1% variation
Q1	NMOS:Si1308EDL、Si1304BDL 1) Drain-Source breakdown voltage \geq 30V 2) Vgs (th) =0.9 (Typ) , 1.3V (Max) 3) Rds on \leq 2.1 Ω @ Vgs=2.5V
L1	47UH/NRH3010T470MN Io = 500 (Max)
CON24Pin	0.5mm ZIF Socket 24Pins,0.5mm pitch

11. Absolute Maximum Rating

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V _{DD}	Logic supply voltage	-0.3 to +6.0	V	-	-	
T _{OPR}	Operation temperature range	0 to 50	°C	35 to70	%	
T _{ttg}	Transportation temperature range	-25 to 60	°C	-	-	Note11-2
T _{stg}	Storage condition	0 to 40	°C	35 to70	%	Maximum storage time: 5 years

Note 11-1:Maximum ratings are those values beyond which damages to the device may occur.

Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

Note11-2: T_{ttg} is the transportation condition, the transport time is within 10 days for -25°C~0°C or 50°C~60°C

12. DC Characteristics

The following specifications apply for: V_{SS}=0V, V_{DD}=3.3V, T_{OPR}=25°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V _{DD}	V _{DD} operation voltage	-	2.5	3.3	3.6	V
V _{IH}	High level input voltage	-	0.7xV _{IO}	-	V _{IO}	V
V _{IL}	Low level input voltage	-	GND	-	0.3xV _{DD}	V
V _{OH}	High level output voltage	I _{OH} = 400 μ A	V _{IO} -0.4	-	-	V
V _{OL}	Low level output voltage	I _{OL} = -400 μ A	GND	-	GND+0.4	V
I _{update}	Module operating current	-	-	3	-	mA
I _{sleep}	Deep sleep mode	V _{CI} =3.3V	-	-	3	μ A



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. The Typical power consumption is measured using associated 25°C waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern.

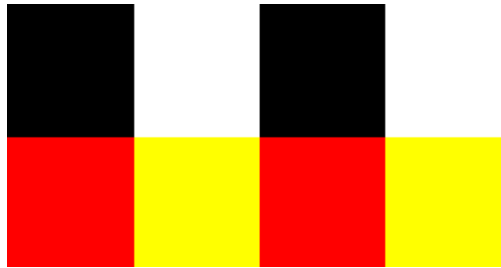
(Note 12-)

- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.

- Vcom value will be OTP before in factory or present on the label sticker.

Note 12-1

The Typical power consumption



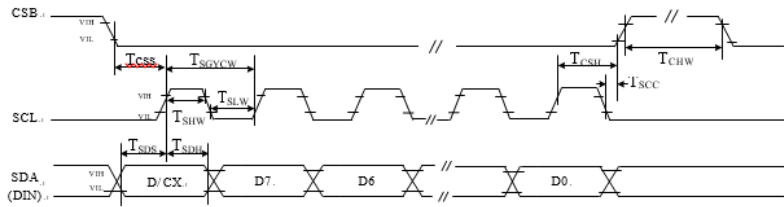
13. Serial Peripheral Interface Timing

The following specifications apply for: VSS=0V, VDD=2.5V to 3.6V, TOPR=25°C

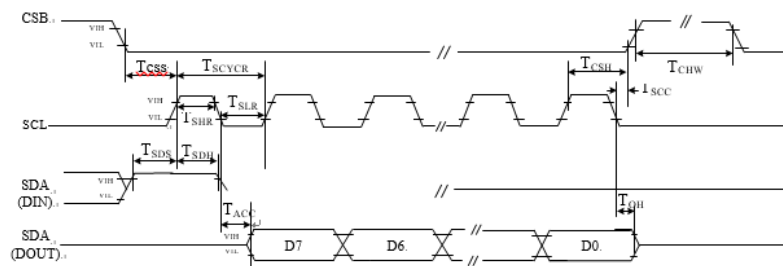
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
SERIAL COMMUNICATION						
CSB	T _{CSS}	60			ns	Chip select setup time
	T _{CSH}	65			ns	Chip select hold time
	T _{SCC}	20			ns	Chip select CSB setup time
	T _{CHW}	40			ns	Chip select setup time
SCL	T _{SCYCW}	100			ns	Serial clock cycle (Write)
	T _{SHW}	35			ns	SCL "H" pulse width (Write)
	T _{SLW}	35			ns	SCL "L" pulse width (Write)
	T _{SCYCR}	150			ns	Serial clock cycle (Read)
	T _{SHR}	60			ns	SCL "H" pulse width (Read)
	T _{SLR}	60			ns	SCL "L" pulse width (Read)
SDA (DIN) (DOUT)	T _{SDS}	30			ns	Data setup time
	T _{SDH}	30			ns	Data hold time
	T _{ACC}			10	ns	Access time
	T _{OH}	15			ns	Output disable time
D/C	T _{DCS}	20			ns	DC setup time
	T _{DCH}	20			ns	DC hold time



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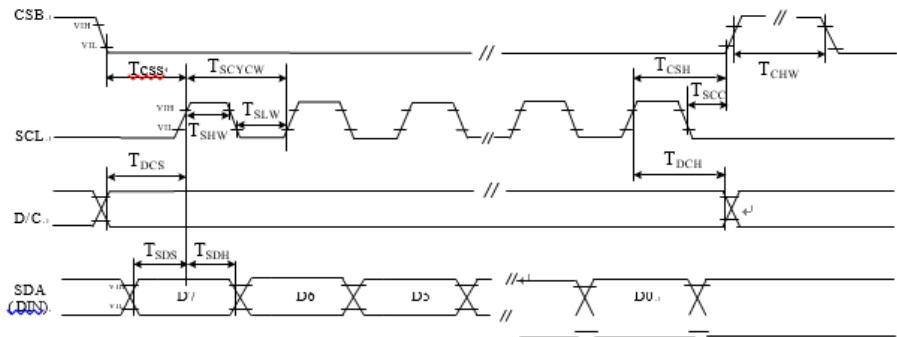


3 pin serial interface characteristics (write mode)¹⁾

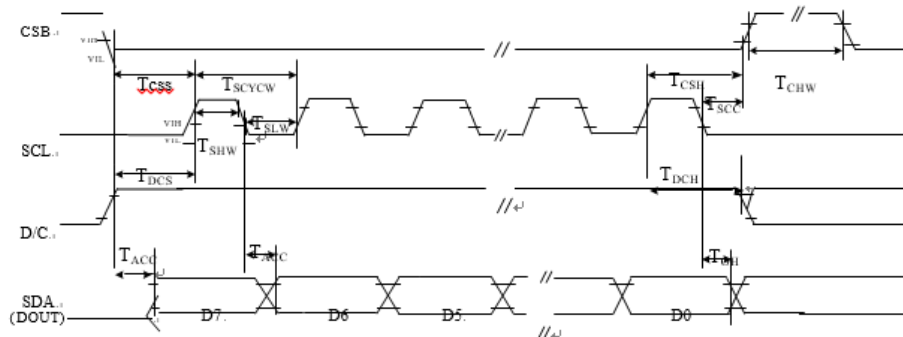


3 pin serial interface characteristics (read mode)¹⁾

V0.1.6¹⁾



4 pin serial interface characteristics (write mode)¹⁾



4 pin serial interface characteristics (read mode)¹⁾

Figure 9: SPI interface timing¹⁾



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14. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25°C	-	60	mAs	-
Peak Current	-	25°C	-	30	mA	
Deep sleep mode	-	25°C	-	3	uA	-

mAs=update average current×update time

15. Optical characteristics

15.1 Specifications

T=25°C ,VDD=3.3V

WS : White state, KS : Black State,

Note 15-1 : Luminance meter : i - One Pro Spectrophotometer

TBD

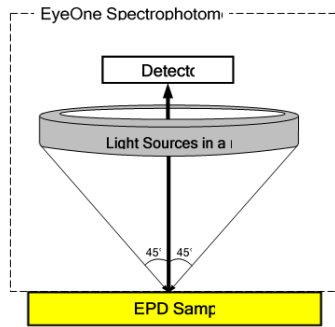
15.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

$$CR = Rl/Rd$$



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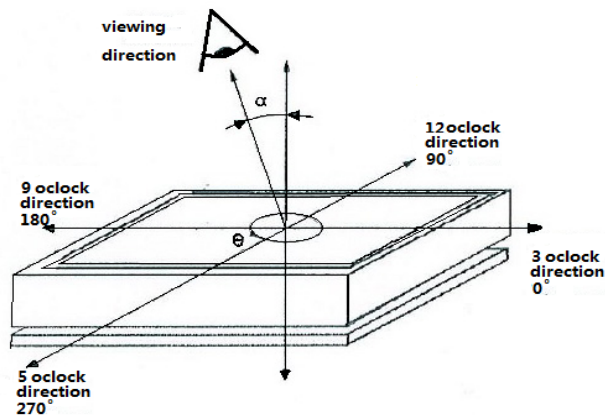


15.3 Reflection Ratio

The reflection ratio is expressed as:

$$R = \text{Reflectance Factor white board} \times (L_{\text{center}} / L_{\text{white board}})$$

L_{center} is the luminance measured at center in a white area ($R=G=B=1$). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.





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16. Handling Safety And Environmental Requirements

WARNING

The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.

Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions

(1) It's recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.

(2) It's recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.

(3) You should adopt radiation structure to satisfy the temperature specification.

(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.

(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)

(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.

(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status

Product specification

The data sheet contains final product specifications.



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Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and does not form part of the specification.

Product Environmental certification
ROHS
REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.



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17. Reliability test

17.1 Reliability test items

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40°C, RH=35%RH, For 240Hr	
2	Low-Temperature Operation	T = 0°C for 240 hrs	
3	High-Temperature Storage	T=60°C RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25°C for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40°C, RH=90%RH, For 168Hr	
6	High Temperature, High-Humidity Storage	T=60°C, RH=80%RH, For 240Hr	Test in white pattern
7	Temperature Cycle	-25°C(30min)~70°C(30min), 100 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment
10	UV exposure Resistance	765 W/m ² for 168hrs,40°C	
11	Electrostatic Discharge(no-operation)	Machine model: +/-250V,0Ω,200pF	

Actual EMC level to be measured on customer application.

Note1: Stay white pattern for storage and non-operation test.

Note2: Operation is black/white pattern , hold time is 150S.

Note3: The function, appearance should meet the requirements of the test before and after the test.

Note4: Keep testing after 2 hours placing at 20°C-25°C.

17.2 Product life time

The EPD Module is designed for a 5-year life-time with 25 °C/50%RH operation assumption. Reliability estimation testing with accelerated life-time theory would be demonstrated to provide confidence of EPD lifetime.

17.3 Product warranty

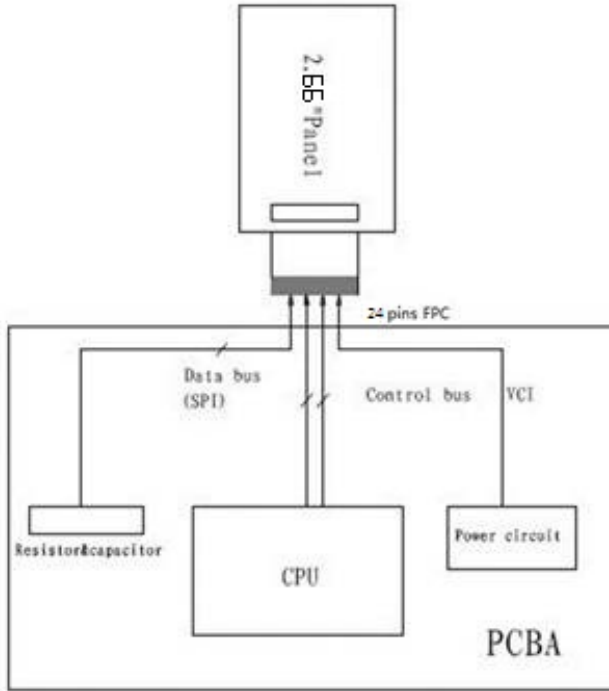
Warranty conditions have to be negotiated between Xingtai and individual customers.

Xingtai provides 12+1(one month delivery time) months warranty for all products which are purchased from Xingtai.

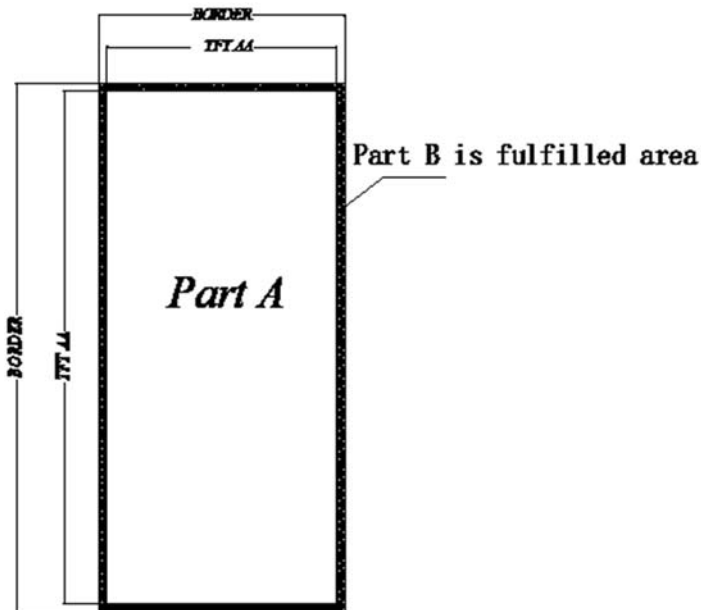


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18. Block Diagram



19. Part A/Part B specification





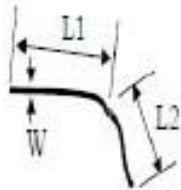
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20. Point and line standard

Shipment Inspection Standard						
Equipment: Electrical test fixture, Point gauge						
Outline dimension	36.3(H)×71.82(V) ×0.95(D)	Unit: mm	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19°C~25°C	55%±5%RH	800~1300Lux	300 mm	35Sec	
Defect type	Inspection method	Standard		Part-A	Part-B	
Spot	Electric Display	D≤0.25 mm		Ignore	Ignore	
		0.25 mm < D ≤ 0.4 mm		N≤4	Ignore	
		D > 0.4 mm		Not Allow	Ignore	
Display unwork	Electric Display	Not Allow		Not Allow	Ignore	
Display error	Electric Display	Not Allow		Not Allow	Ignore	
Scratch or line defect(include dirt)	Visual/Film card	L≤2 mm, W≤0.2 mm		Ignore	Ignore	
		2.0mm < L ≤ 5.0mm, 0.2 < W ≤ 0.3mm,		N≤2	Ignore	
		L > 5 mm, W > 0.3 mm		Not Allow	Ignore	
PS Bubble	Visual/Film card	D≤0.2mm		Ignore	Ignore	
		0.2mm ≤ D ≤ 0.35mm & N≤4		N≤4	Ignore	
		D > 0.35 mm		Not Allow	Ignore	
Side Fragment	Visual/Film card	X≤6mm, Y≤0.4mm, Do not affect the electrode circuit (Edge chipping)				
		X≤1mm, Y≤1mm, Do not affect the electrode circuit((Corner chipping)				
		Ignore				
						
Remark	1. Appearance defect should not cause electrical defects					
	2. Appearance defects should not cause dimensional accuracy problems					
	L=long W=wide D=point size N=Defects NO					

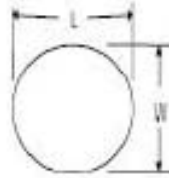


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$$L = L1 + L2$$

Line Defect



$$D = (L + W) / 2$$

Spot Defect

L=long W=wide D=point size



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21. Barcode

The printed QR code is shown as below



What is the QR code after picture being scanned and read? It consist of 30 numbers and letters, here is explanation for it.

QR Code: ABBBBBBBBBBFFCCDDDEEEEGHIJKLL

- ① A means Factory code, eg: H(HINK)
- ② BBBBBBBBBB refers to product model name, which is in consistent with specification part number.eg:E0213A189 or E0266A120; When the total code is less than 9, it would be added suffix with **. eg: E027A45** or E0154A78*
- ③ FF means production workshop
- ④ CCC means date of production
- ⑤ DDD means production batch
- ⑥ EEEE means FPL lot
- ⑦ G means MP/Sample/Trial/Repair
- ⑧ HIJ:(H——TFT;I——PS;J——EC Glue)
- ⑨ KK means IC type
- ⑩ LL means serial number



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22. Packing

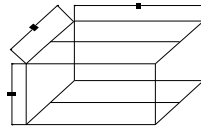
Packing Spec

Sheet No:

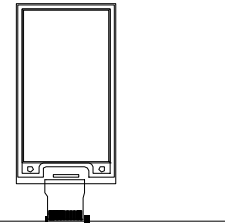
Part No	HINK-E0266A**	DATE	2020.07.22	VER	A0	Page	1-1
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一, Package Type: Box

Box No	Holitech shipping box
Box size	515*322*170
Containment	288PCS

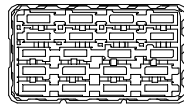


PRODUCT DRAWING



二, Inside package type: Plastic Tray
Tray unit: mm

Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE (inside)	408.86*231.5*2	12 pcs
EPE (Up-Down)	485*145*10	2 pcs
EPE (Left-Right)	285*480*10	2 pcs
EPE (Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	24 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	

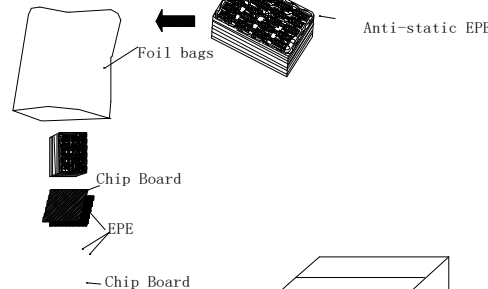


Step 1:
Material: Tray, EPE
Put the product in to the tray and keep the display side up. Then put anti-static EPE in to each holes.

Step 2:
1) Must keep the angle 180 degree placed between the neighboring Plastic trays.
2) There are 12 layers product, total 24*12=288 pcs.
3) An empty Plastic tray intersects put on the top of the plastic trays.

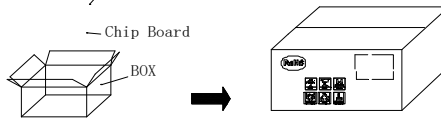
Step 3:

- 1) In each case, put 2 bags of desiccant, then seal the trays with adhesive tapes.
- 2) Put the trays into foil bags.
- 3) heat seal the foil bags.



Step 4:

- 1) First put a chip board on the bottom of the box, then placed the down EPE, the left - right and front -back EPE.
- 2) Placed the sealed products into the box.
- 3) The last placed the up EPE on the top of the trays, and place a chip board on it.



Step 5:

- 1) Seal the box with adhesive tapes .
- 2) Paste the lable onto the exterior box, and the lable can't cover the safety , transfer and RoSH sign.

Design	Z. Z. Q	Approve	H. Z. P	Confirm	X.X.M
Date	2020.07.22	Date	2020.07.22	Date	2020.07.22