KARO electronics

NEW

QS Family
QFN Style Solder-Down
Computer-on-Modules

- Solder-down version
- 27mm square
- 2.3mm total height
- QFN type lead style
  - 1mm pitch
  - 100 pads
  - Thermal pad
- Visual solder joint inspection possible after soldering
- Single-sided assembly
- High speed design compliant
- 3.3V power supply

Key Features

• Processor	STM32MP1 Series
	Arm® Cortex®-A7 650MHz
	Arm® Cortex®-M4 209MHz
• RAM	256MB or 512MB DDR3L
• ROM	4GB eMMC or 128MB SLC NAND
• Grade	Industrial
• Temperature	-25°C to 85°C (eMMC)
	-40°C to 85°C (NAND)
• Display support	
Display Interface	24-bit RGB
	MIPI® DSI (2-lanes)*⁾
GPU*⁾	3D GPU: Vivante®,
	OpenGL® ES 2.0
• Connectivity	

- Connectivity
  - Gb Ethernet, USB2.0, eMMC/SD
  - UART, I²C, SPI, PWM, SAI, CAN*⁾

OS Support

- Linux

*) Depends on SPM32MP1 version

Dual Cortex®-A7

ST life.augmented

Authorized Partner

Ka-Ro electronics GmbH - Pascalstr. 22, D-52076 Aachen, Germany - Tel.: +49 2408 1402-0 (FAX -10)

www.karo-electronics.de

STM32MP1 Block Diagram

ARM® Dual Cortex®-A7 650 MHz
- L1 32kB I
- L1 32kB D
- 256kB L2 Cache

ARM® Cortex®-M4 209 MHz
- FPU
- MPU

External Memories
- 3x SDMMC
- Dual Quad-SPI
- DDR3L @ 533 Mhz

Internal Memories
- OTP fuse 3kB
- System RAM 256kB
- Backup RAM 4kB
- MCU System RAM 384kB
- MCU Retention RAM 64kB

Graphics
- LCD-TFT controller
- MIPI-DSI controller
- 3D GPU OpenGL ES 2.0 @ 533 MHz

Control
- 15x 16-bit timers
- 2x 32-bit timers
- 2x 16-bit advanced motor control timers

Connectivity
- 10/100M or Gigabit Ethernet GMAC
- Camera interface
- HDMI-CEC
- 3x USB 2.0 Host/OTG with 2x HS PHY
- DFSDM (8 channels/6 filters)
- MDIO slave
- 6x SPI / 3x I²S
- 6x I²C
- 4x UART + 4x USART
- 4x SAI
- SPDIF
- 2x CAN FD

Analog
- 2x 16-bit ADCs
- 2x 12-bit DACs

Security
- TrustZone
- SHA-256, MD5, HMAC
- 3x Tamper Pins with 1 active
- Secure RAMs
- Secure Peripherals
- Secure RTC
- Analog true RNG
- 96-bit unique ID
- AES 256, TDES
- Secure Boot

System
- 5x LDOs
- Internal and External Oscillators
- MDMA + 2x DMA
- Reset and Clock
- 3x watchdogs
- Up to 176 GPIOs

STM32 MP157 only
n/a on STM32 MP151
STM32 MP15xC only

|	QSMP-1510 STM32MP151A	QSMP-1510C STM32MP157C	QSMP-1530C STM32MP157C	QSMP-1570 STM32MP157C
Primary Arm® Core	1x Cortex®-A7 up to 650 MHz	2x Cortex®-A7 up to 650 MHz	2x Cortex®-A7 up to 650 MHz	
Secondary Arm® Core	1x Cortex-M4 up to 200 MHz	1x Cortex-M4 up to 200 MHz	1x Cortex-M4 up to 200 MHz	
RAM	256 MB		256 MB	512 MB
ROM	128MB SLC NAND		4GB eMMC	
Display Interface	24-bit RGB		24-bit RGB + 2-lane MIPI-DSI	
3D GPU	-	yes	yes	
CAN	-	2x FD-CAN	2x FD-CAN	
Security	-	Secure Boot, Cryptography		
Temperature	-40°C to 85°C	-40°C to 85°C	-25°C to 85°C	
Order Code	QSMP/151A/256S/128F/I	QSMP/157C/256S/128F/I	QSMP/157C/256S/4GF/E85	QSMP/157C/512S/4GF/E85

QFN Style Computer On Module Advantages

Defined Return Path

The reason PCB layout becomes more and more important is because of the trend to faster, higher integrated, smaller formfactors, and lower power electronic circuits. The higher the switching frequencies are, the more radiation may occur on a PCB. With good layout, many EMI problems can be minimized to meet the required specifications.

When a module or component is used in a design, the supplier specifies the basis for such a layout. It's not only the pinout which should lead to an easy wiring without the need for crossings. He has also provide a proper solution for the signal path back to the module. If this return path, mostly the ground plane, cannot be connected near the signal pin, the return current has to take another way and this may result in a loop area. The larger the area, the more radiation and EMI problems may occur.

Ka-Ro QSCOM modules uses a large ground pad on the bottom side. With this a defined ground plane connection is available for all signals. In addition to have a good return path for all signals this large ground pad can be used for cooling.
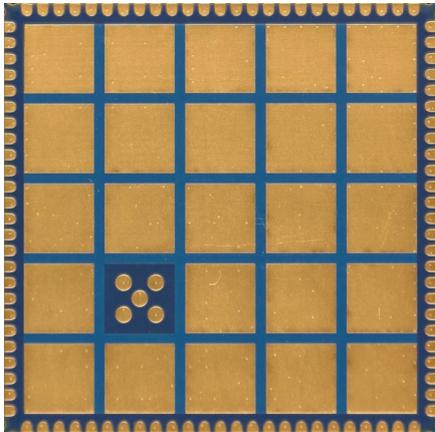

Easy Wiring - Even 2-layer printed circuit boards can be used.

With a solid ground plane on the bottom layer, high speed signals can be routed on the top layer at a defined impedance. However, this is only possible if a peripheral or plug can be connected directly without crossing the routing.

Advanced Soldering

Using a large solder pad underneath the component has not only electrical and thermal advantages. This is also used to hold the component at a defined height during soldering, without the solder being compressed by the weight, which could result in short circuits.

Standard Contact Assignments

Ka-Ro electronics GmbH - Pascalstr. 22, D-52076 Aachen, Germany - Tel.: +49 2408 1402-0 (FAX -10)

www.karo-electronics.de
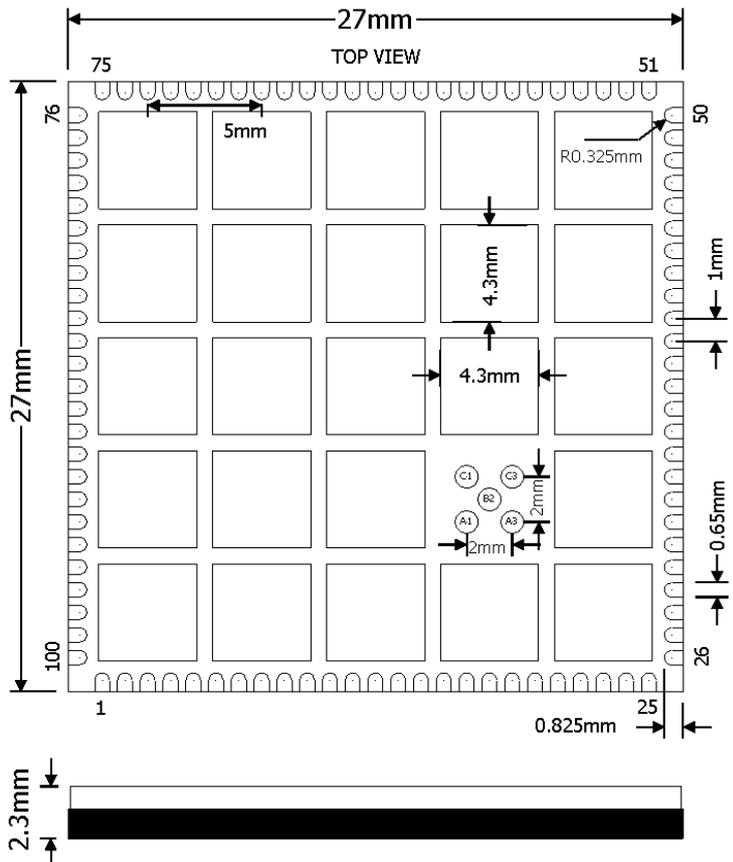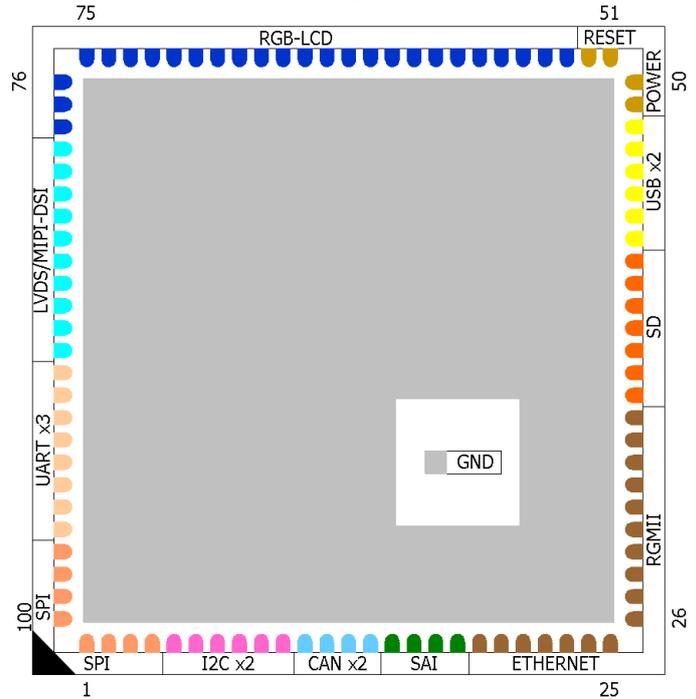
Layout Guidelines

Land pattern
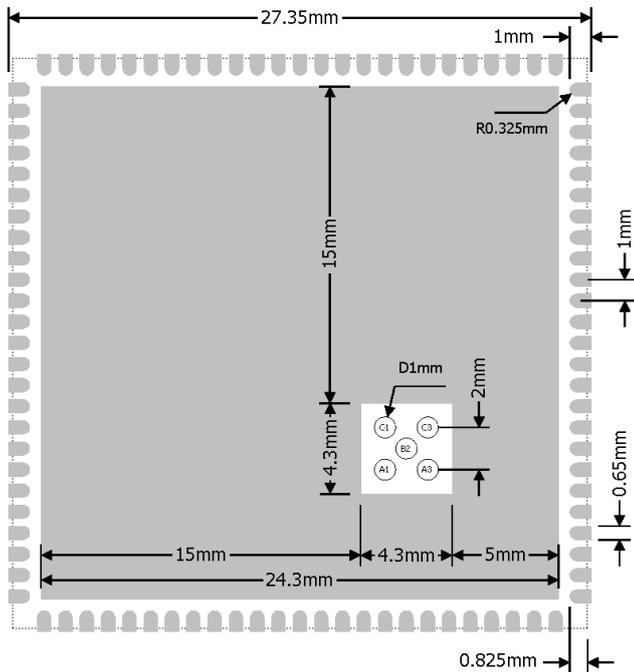
See figure above for the suggested module layout. The five 1mm pads in the square GND pad cutout can be omitted if no JTAG Boundary Scan test is used. The solder mask openings are shown below.
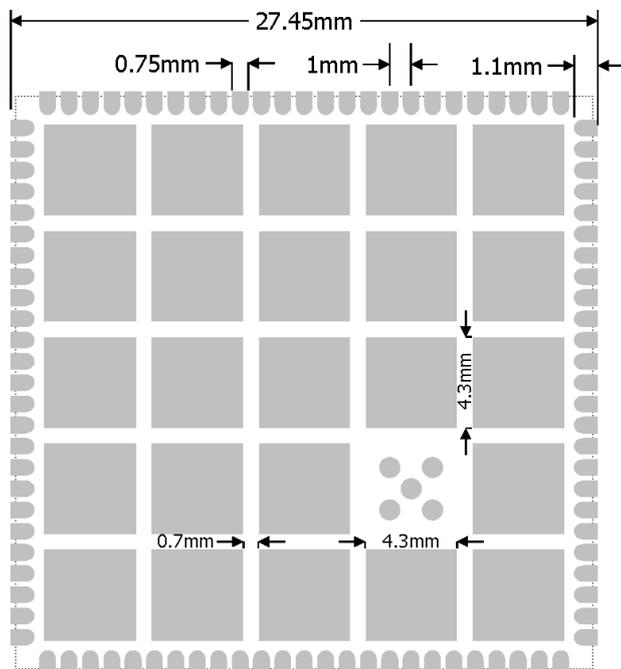
The ground pad solder mask on the bottom side of the QSCOM module is divided into sections for a better reliability of the solder joint and self-alignment of the component.

If the via holes used on the application board have a diameter larger than 0.3 mm, it is recommended to mask the via holes to prevent solder wicking through the via holes. Solders have a habit of filling holes and leaving voids in the thermal pad solder junction, as well as forming solder balls on the other side of the application board which can in some cases be problematic. The 0.7mm wide solder mask stripes can be used to arrange the vias as shown here:
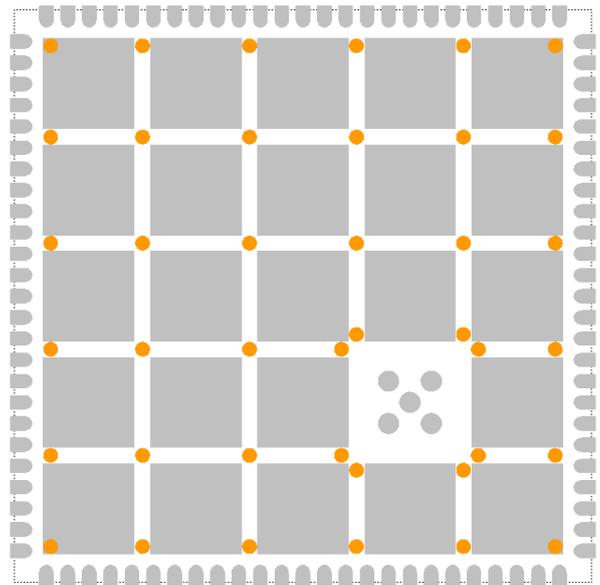
Soldering Recommendations

Ka-Ro QSCOM modules are compatible with industrial standard reflow profile for Pb-free solders. Ka-Ro will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendations should be taken as a starting point guide.

- Refer to technical documentations of particular solder paste for reflow profile configurations
- Avoid using more than one flow.
- A 150µm stencil thickness is recommended.
- Aperture size of the stencil should be 1:1 with the pad size.
- A low residue, "no clean" solder paste should be used due to low mounted height of the component.

Recommended stencil design
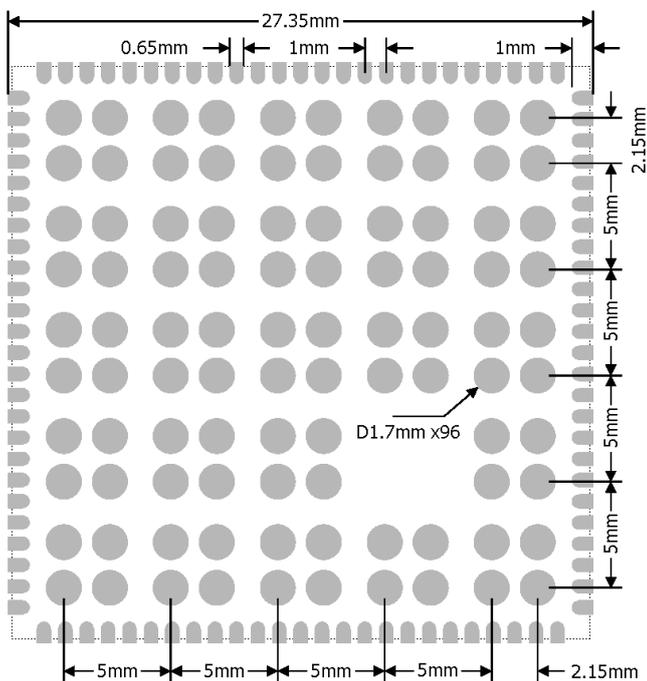
Aperture size of the stencil is 1:1 with the pad size. Four 1.7mm diameter bumps are used for each of the 4.3mm square GND pads sections giving a 50% solder paste padding. The lower component settling with this ensures that the pads at the edge are always soldered even at vertical misalignment by distortion or warping.

Thermal Considerations

The QSCOM module consume more than 1 W of DC power. In any application where high ambient temperatures for more than a few seconds can occur, it is important that a sufficient cooling surface is provided to dissipate the heat. The thermal pad at the bottom of the module must be connected to the application board ground planes by soldering. The application board should provide a number of vias under and around the pad to conduct the produced heat to the board ground planes, and preferably to a copper surface on the other side of the board in order to conduct and spread the heat. The module internal thermal resistance should in most cases be negligible compared to the thermal resistance from the module into air, and common equations for surface area required for cooling can be used to estimate the temperature rise of the module. Only copper planes on the circuit board surfaces with a solid thermal connection to the module ground pad will dissipate heat. For an application with high load the maximum allowed ambient temperature should be reduced due to inherent heating of the module, especially with small fully plastic enclosed applications where heat transfer to ambient air is low due to low thermal conductivity of plastic. The module measured on the evaluation board exhibits a temperature rise of about 20°C above ambient temperature. An insufficiently cooled module will rapidly heat beyond operating range in ambient room temperature.

Packaging

Section Y-Y

	Ao	27.59	+/-	0.1
	Bo	27.59	+/-	0.1
	Ko	2.72	+/-	0.1
	F	20.20	+/-	0.15
	P1	32.00	+/-	0.1
	So	40.40	+/-	0.1
	W	44.00	+/-	0.3

MATERIAL: CONDUCTIVE POLYSTYRENE (IV)

DRAWN: Rajesh   GENERAL TOLERANCE: ±0.2

DRAWING NO: CP216/01-0   SCALE: NTS

TITLE: OPEN TOOL EMBOSSED CARRIER TAPE DIMENSIONS
BGA 2727/5

C-PAK PTE LTD

THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO C-PAK PTE.LTD.

REV	DESCRIPTION	DATE	APPROVED
0	NEW DRAWING	24.10.01	MAT

1st Angle
3rd Angle
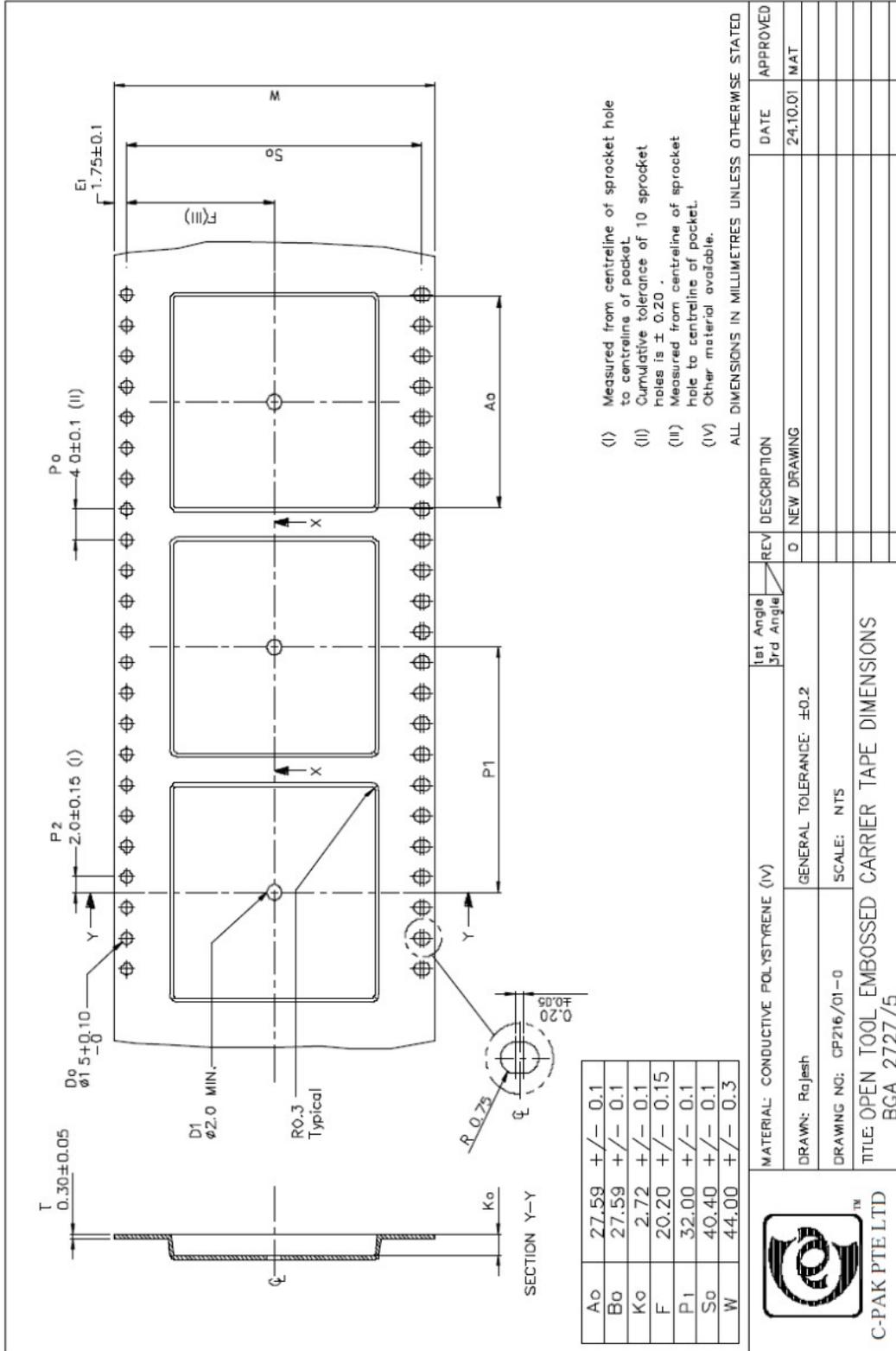
(I)   Measured from centreline of sprocket hole to centreline of pocket.
(II)   Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV)   Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

PINOUT (STM32MP1 pads named PA, PB, etc. can be used as GPIO ports)

PIN	QSCOM STANDARD	MP1 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
1st SPI							
1	SPIA_NSS	PE11	- TIM1_CH2 - DFSDM1_CKIN4	- **SPI4_NSS** - USART6_CK	- - SAI2_SD_B -	FMC_D8/FMC_DA8 DCMI_D4 LCD_G3 EVENTOUT	
2	SPIA_MISO	PE5	TRACED3 - SAI1_CK2 DFSDM1_CKIN3	- **SPI4_MISO** SAI1_SCK_A SDMMC2_D0DIR	SDMMC1_D0DIR SDMMC2_D6 - SDMMC1_D6	FMC_A21 DCMI_D6 LCD_G0 EVENTOUT	
3	SPIA_MOSI	PE14	- TIM1_CH4 - -	- **SPI4_MOSI** - -	UART8_RTS/UART8_DE - SAI2_MCLK_B SDMMC1_D123DIR	FMC_D11/FMC_DA11 LCD_G0 LCD_CLK EVENTOUT	
4	SPIA_SCK	PE2	TRACECLK - SAI1_CK1 -	I2C4_SCL **SPI4_SCK** SAI1_MCLK_A -	- QUADSPI_BK1_IO2 - ETH1_RGMII_TXD3	FMC_A23 - - EVENTOUT	
I2C							
5	I2CA_SCL	PA11	- TIM1_CH4 **I2C6_SCL** -	I2C5_SCL SPI2_NSS/I2S2_WS UART4_RX USART1_CTS/USART1_NSS	- FDCAN1_RX - -	- - LCD_R4 EVENTOUT	
6	I2CA_SDA	PA12	- TIM1_ETR **I2C6_SDA** -	I2C5_SDA - UART4_TX USART1_RTS/USART1_DE	SAI2_FS_B FDCAN1_TX - -	- - LCD_R5 EVENTOUT	
7	INTA	**PD12**	- LPTIM1_IN1 TIM4_CH1 LPTIM2_IN1	I2C4_SCL I2C1_SCL - USART3_RTS/USART3_DE	- QUADSPI_BK1_IO1 SAI2_FS_A -	FMC_ALE/FMC_A17 - - EVENTOUT	
8	I2CB_SCL	PZ0	- - I2C6_SCL **I2C2_SCL**	- SPI1_SCK/I2S1_CK - USART1_CK	SPI6_SCK - - -	- - - EVENTOUT	
9	I2CB_SDA	PZ1	- - I2C6_SDA **I2C2_SDA**	I2C5_SDA SPI1_MISO/I2S1_SDI I2C4_SDA USART1_RX	SPI6_MISO - - -	- - - EVENTOUT	
10	INTB	**PF15**	TRACED7 - - -	I2C4_SDA I2C1_SDA - -	- - - ETH1_GMII_RXD7	FMC_A9 - - EVENTOUT	
CAN							
11	CANA_RX	PD0	- - I2C6_SDA DFSDM1_CKIN6	I2C5_SDA - SAI3_SCK_A -	UART4_RX **FDCAN1_RX** SDMMC3_CMD DFSDM1_DATIN7	FMC_D2/FMC_DA2 - - EVENTOUT	
12	CANA_TX	PD1	- - I2C6_SCL DFSDM1_DATIN6	I2C5_SCL - SAI3_SD_A -	UART4_TX **FDCAN1_TX** SDMMC3_D0 DFSDM1_CKIN7	FMC_D3/FMC_DA3 - - EVENTOUT	
13	CANB_RX	PB5	ETH_CLK TIM17_BKIN TIM3_CH2 SAI4_D1	I2C1_SMBA SPI1_MOSI/I2S1_SDO I2C4_SMBA SPI3_MOSI/I2S3_SDO	SPI6_MOSI **FDCAN2_RX** SAI4_SD_A ETH1_PPS_OUT	UART5_RX DCMI_D10 LCD_G7 EVENTOUT	
14	CANB_TX	PB13	- TIM1_CH1N - DFSDM1_CKOUT	LPTIM2_OUT SPI2_SCK/I2S2_CK DFSDM1_CKIN1 USART3_CTS/USART3_NSS	- **FDCAN2_TX** - ETH1_RGMII_TXD1	- - UART5_TX EVENTOUT	
SAI							
15	SAI_TX	PD11	- - - LPTIM2_IN2	I2C4_SMBA I2C1_SMBA - USART3_CTS/USART3_NSS	QUADSPI_BK1_IO0 - **SAI2_SD_A** -	FMC_CLE/FMC_A16 - - EVENTOUT	
16	SAI_RX	PA0	- TIM2_CH1/TIM2_ETR TIM5_CH1 TIM8_ETR	TIM15_BKIN - - USART2_CTS/USART2_NSS	UART4_TX SDMMC2_CMD **SAI2_SD_B** CRS/ETH1_MII_CRS	- - - EVENTOUT	ADC1_INP16, WKUP1
17	SAI_SCK	PD13	- LPTIM1_OUT TIM4_CH2 -	I2C4_SDA I2C1_SDA I2S3_MCK -	- QUADSPI_BK1_IO3 **SAI2_SCK_A** -	FMC_A18 DSI_TE - EVENTOUT	

PIN	QSCOM STANDARD	MP1 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
18	SAI_FS	PI7	- - - TIM8_CH3	- - - -	- - **SAI2_FS_A** -	DCMI_D7 LCD_B7 EVENTOUT	
ETHERNET							
19	ENET_RST	**PA4**	HDP0 - TIM5_ETR -	SAI4_D2 SPI1_NSS/I2S1_WS SPI3_NSS/I2S3_WS USART2_CK	SPI6_NSS - - -	SAI4_FS_A DCMI_HSYNC LCD_VSYNC EVENTOUT	ADC1_INP18, ADC2_INP18, DAC_OUT1
20	ENET_CK125	PG5	TIM1_ETR - - -	- - - -	- - - **ETH1_RGMII_CLK125**	FMC_A15 - - EVENTOUT	
21	ENET_INT	**PA9**	- TIM1_CH2 - -	I2C3_SMBA SPI2_SCK/I2S2_CK - USART1_TX	SDMMC2_CDIR - SDMMC2_D5 -	- DCMI_D0 LCD_R5 EVENTOUT	
22	ENET_MDIO	PA2	- TIM2_CH3 TIM5_CH3 LPTIM4_OUT	TIM15_CH1 - - USART2_TX	SAI2_SCK_B - SDMMC2_D0DIR **ETH1_MDIO**	MDIOS_MDIO - LCD_R1 EVENTOUT	ADC1_INP14, WKUP2
23	ENET_MDC	PC1	TRACED0 - SAI1_D1 DFSDM1_DATIN0	DFSDM1_CKIN4 SPI2_MOSI/I2S2_SDO SAI1_SD_A -	- SDMMC2_CK - **ETH1_MDC**	MDIOS_MDC - - EVENTOUT	ADC1_INP11, ADC1_INN10, ADC2_INP11, ADC2_INN10, TAMP_IN3, WKUP6
24	ENET_RXC	PA1	ETH_CLK TIM2_CH2 TIM5_CH2 LPTIM3_OUT	TIM15_CH1N - - USART2_RTS/USART2_DE	UART4_RX QUADSPI_BK1_IO3 SAI2_MCLK_B **ETH1_RGMII_RX_CLK**/ ETH1_RMII_REF_CLK	- - LCD_R2 EVENTOUT	ADC1_INP17, ADC1_INN16
25	ENET_RX_CTL	PA7	- TIM1_CH1N TIM3_CH2 TIM8_CH1N	SAI4_D1 SPI1_MOSI/I2S1_SDO - -	SPI6_MOSI TIM14_CH1 QUADSPI_CLK **ETH1_RGMII_RX_CTL**/ ETH1_RMII_CRS_DV	SAI4_SD_A - - EVENTOUT	ADC1_INP7, ADC1_INN3, ADC2_INP7, ADC2_INN3
26	ENET_RXD0	PC4	- - - DFSDM1_CKIN2	I2S1_MCK - - -	SPDIFRX_IN2 - **ETH1_RGMII_RXD0**/ ETH1_RMII_RXD0	- - - EVENTOUT	ADC1_INP4, ADC2_INP4
27	ENET_RXD1	PC5	- - SAI1_D3 DFSDM1_DATIN2	SAI4_D4 SAI1_D4 - -	SPDIFRX_IN3 - **ETH1_RGMII_RXD1**/ ETH1_RMII_RXD1	SAI4_D3 - - EVENTOUT	ADC1_INP8, ADC1_INN4, ADC2_INP8, ADC2_INN4
28	ENET_RXD2	PB0	- TIM1_CH2N TIM3_CH3 TIM8_CH2N	- - DFSDM1_CKOUT -	UART4_CTS LCD_R3 - **ETH1_RGMII_RXD2**	MDIOS_MDIO - LCD_G1 EVENTOUT	ADC1_INP9, ADC1_INN5, ADC2_INP9, ADC2_INN5
29	ENET_RXD3	PH7	- - - -	I2C3_SCL SPI5_MISO - -	- - - **ETH1_RGMII_RXD3**	MDIOS_MDC DCMI_D9 - EVENTOUT	
30	ENET_TX_CTL	PB11	- TIM2_CH4 - LPTIM2_ETR	I2C2_SDA - DFSDM1_CKIN7 USART3_RX	- - - **ETH1_RGMII_TX_CTL**/ ETH1_RMII_TX_EN	- DSI_TE LCD_G5 EVENTOUT	
31	ENET_TXC	PG4	- TIM1_BKIN2 - -	- - - -	- - - **ETH1_RGMII_GTX_CLK**	FMC_A14 - - EVENTOUT	
32	ENET_TXD3	PB8	HDP6 TIM16_CH1 TIM4_CH3 DFSDM1_CKIN7	I2C1_SCL SDMMC1_CKIN I2C4_SCL SDMMC2_CKIN	UART4_RX FDCAN1_RX SDMMC2_D4 **ETH1_RGMII_TXD3**	SDMMC1_D4 DCMI_D6 LCD_B6 EVENTOUT	
33	ENET_TXD2	PC2	- - - DFSDM1_CKIN1	SPI2_MISO/I2S2_SDI DFSDM1_CKOUT -	- - - **ETH1_RGMII_TXD2**	DCMI_PIXCLK - EVENTOUT	ADC1_INP12, ADC1_INN11

PIN	QSCOM STANDARD	MP1 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
34	ENET_TXD1	PG14	TRACED1 LPTIM1_ETR - -	- SPI6_MOSI SAI4_D1 USART6_TX	- QUADSPI_BK2_IO3 SAI4_SD_A **ETH1_RGMII_TXD1**/ ETH1_RMII_TXD1	FMC_A25 - LCD_B0 EVENTOUT	
35	ENET_TXD0	PG13	TRACED0 LPTIM1_OUT SAI1_CK2 -	SAI4_CK1 SPI6_SCK SAI1_SCK_A USART6_CTS/USART6_NSS	- - SAI4_MCLK_A **ETH1_RGMII_TXD0**/ ETH1_RMII_TXD0	FMC_A24 - LCD_R0 EVENTOUT	
SD							
36	SD_CD	**PB7**	- TIM17_CH1N TIM4_CH2 -	I2C1_SDA - I2C4_SDA USART1_RX	- - SDMMC2_D1 DFSDM1_CKIN5	FMC_NL DCMI_VSYNC - EVENTOUT	
37	SD_D1	PC9	TRACED1 - TIM3_CH4 TIM8_CH4	I2C3_SDA I2S_CKIN - -	UART5_CTS QUADSPI_BK1_IO0 - -	**SDMMC1_D1** DCMI_D3 LCD_B2 EVENTOUT	
38	SD_D0	PC8	TRACED0 - TIM3_CH3 TIM8_CH3	- - UART4_TX USART6_CK	UART5_RTS/UART5_DE - - -	**SDMMC1_D0** DCMI_D2 - EVENTOUT	
39	SD_CLK	PC12	TRACECLK MCO2 SAI4_D3 -	- SPI3_MOSI/I2S3_SDO USART3_CK	UART5_TX - SAI4_SD_B -	**SDMMC1_CK** DCMI_D9 - EVENTOUT	
40	SD_CMD	PD2	- TIM3_ETR - -	I2C5_SMBA UART4_RX	UART5_RX - - -	**SDMMC1_CMD** DCMI_D11 - EVENTOUT	
41	SD_D3	PC11	TRACED3 - DFSDM1_DATIN5	- SPI3_MISO/I2S3_SDI USART3_RX	UART4_RX QUADSPI_BK2_NCS SAI4_SCK_B -	**SDMMC1_D3** DCMI_D4 - EVENTOUT	
42	SD_D2	PC10	TRACED2 - DFSDM1_CKIN5	- - SPI3_SCK/I2S3_CK USART3_TX	UART4_TX QUADSPI_BK1_IO1 SAI4_MCLK_B -	**SDMMC1_D2** DCMI_D8 LCD_R2 EVENTOUT	
USB							
43	USBA_VBUS		Not connected				
44	USBA_DN	USB_DM1					
45	USBA_DP	USB_DP1					
46	USBB_VBUS	OTG_VBUS					
47	USBB_DN	USB_DM2					
48	USBB_DP	USB_DP2					
POWER SUPPLY & RESET							
49	VIN		3.3V power supply input				
50							
51	NRST_PWREN		This dual function pin is used as reset input and peripheral power supply enable output. NRST_PWREN is directly connected to STM32MP1 NRST and NRST_CORE and enables the DDR memory power supply VDD_DDR. 10nF capacitors on NRST and NRST_CORE protects the device against parasitic resets. The STM32MP1 has permanent internal pull-up resistors to 3.3V. Refer also to STM32MP1 datasheet, chap. 6.3.18 NRST and NRST_CORE pin characteristics.				
52	BOOT_MODE						H: Boot from FLASH L: Boot from UART/USB
DISPLAY							
53	**LCD_DE** CSI_DP2 LVDS1_TX2P	PE13	HDP2 TIM1_CH3 - DFSDM1_CKIN5	- SPI4_MISO - -	- - SAI2_FS_B -	FMC_D10/FMC_DA10 DCMI_D6 **LCD_DE** EVENTOUT	
54	**LCD_VSYNC** CSI_DN2 LVDS1_TX2N	PI9	HDP1 - - -	- - - -	UART4_RX FDCAN1_RX - -	- - **LCD_VSYNC** EVENTOUT	
55	**LCD_HSYNC** CSI_DP0 LVDS1_TX0P	PI10	HDP0 - - -	- - - -	USART3_CTS/USART3_NSS - - ETH1_GMII_RX_ER/ ETH1_MII_RX_ER	- - **LCD_HSYNC** EVENTOUT	

PIN	QSCOM STANDARD	MP1 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
56	**LCD_CLK** CSI_DN0 LVDS1_TX0N	PG7	TRACED5 - -	- SAI1_MCLK_A USART6_CK	UART8_RTS/UART8_DE QUADSPI_CLK - QUADSPI_BK2_IO3	DCMI_D13 **LCD_CLK** EVENTOUT	
57	**LCD_R1** CSI_CKN LVDS1_CLKN	PH3	- - CKIN4	- - -	QUADSPI_BK2_IO1 SAI2_MCLK_B ETH1_GMII_COL/ ETH1_MII_COL	- **LCD_R1** EVENTOUT	
58	**LCD_R2** CSI_DP1 LVDS1_TX1P	PH8	- TIM5_ETR -	I2C3_SDA - -	- - -	DCMI_HSYNC **LCD_R2** EVENTOUT	
59	**LCD_R3** CSI_DN1 LVDS1_TX1N	PH9	- TIM12_CH2 -	I2C3_SMBA	-	DCMI_D0 **LCD_R3** EVENTOUT	
60	**LCD_R4** CSI_DP3 LVDS1_TX3P	PH10	- TIM5_CH1	I2C4_SMBA I2C1_SMBA	-	DCMI_D1 **LCD_R4** EVENTOUT	
61	**LCD_R5** CSI_DN3 LVDS1_TX3N	PH11	- TIM5_CH2	I2C4_SCL I2C1_SCL	-	DCMI_D2 **LCD_R5** EVENTOUT	
62	**LCD_R6** DSI_DP2 LVDS0_TX2P	PH12	HDP2 TIM5_CH3	I2C4_SDA I2C1_SDA	-	- DCMI_D3 **LCD_R6** EVENTOUT	
63	**LCD_R7** DSI_DN2 LVDS0_TX2N	PE15	HDP3 TIM1_BKIN -	TIM15_BKIN - USART2_CTS/USART2_NSS	UART8_CTS - FMC_NCE2	FMC_D12/FMC_DA12 - **LCD_R7** EVENTOUT	
64	**LCD_G2**	PH13	- - TIM8_CH1N	-	UART4_TX FDCAN1_TX	- **LCD_G2** EVENTOUT	
65	**LCD_G3**	PH14	- - TIM8_CH2N	-	UART4_RX FDCAN1_RX	DCMI_D4 **LCD_G3** EVENTOUT	
66	**LCD_G4**	PH15	- - TIM8_CH3N	-	-	DCMI_D11 **LCD_G4** EVENTOUT	
67	**LCD_G5**	PI0	- TIM5_CH4	SPI2_NSS/I2S2_WS - -	-	DCMI_D13 **LCD_G5** EVENTOUT	
68	**LCD_G6**	PI1	- TIM8_BKIN2	SPI2_SCK/I2S2_CK	-	DCMI_D8 **LCD_G6** EVENTOUT	
69	**LCD_G7**	PI2	- - TIM8_CH4	SPI2_MISO/I2S2_SDI	-	DCMI_D9 **LCD_G7** EVENTOUT	
70	**LCD_B1**	PG12	LPTIM1_IN1 - -	SPI6_MISO SAI4_CK2 USART6_RTS/USART6_DE	SPDIFRX_IN1 LCD_B4 SAI4_SCK_A ETH1_PHY_INTN	FMC_NE4 - **LCD_B1** EVENTOUT	
71	**LCD_B2**	PG10	TRACED10 - -	-	UART8_CTS LCD_G3 SAI2_SD_B QUADSPI_BK2_IO2	FMC_NE3 DCMI_D2 **LCD_B2** EVENTOUT	
72	**LCD_B3**	PD10	RTC_REFIN TIM16_BKIN - DFSDM1_CKOUT	I2C5_SMBA SPI3_MISO/I2S3_SDI SAI3_FS_B USART3_CK	-	FMC_D15/FMC_DA15 - **LCD_B3** EVENTOUT	
73	**LCD_B4**	PI4	- - TIM8_BKIN	-	- - SAI2_MCLK_A	DCMI_D5 **LCD_B4** EVENTOUT	
74	**LCD_B5**	PI5	- TIM8_CH1	-	- - SAI2_SCK_A	DCMI_VSYNC **LCD_B5** EVENTOUT	
75	**LCD_B6**	PI6	- - TIM8_CH2	-	- - SAI2_SD_A	DCMI_D6 **LCD_B6** EVENTOUT	

PIN	QSCOM STANDARD	MP1 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
76	**LCD_B7**	PD8	- - - DFSDM1_CKIN3	- - SAI3_SCK_B USART3_TX	- SPDIFRX_IN1 - -	FMC_D13/FMC_DA13 - **LCD_B7** EVENTOUT	
Display Control							
77	**LCD_EN**	**PA10**	TIM1_CH3 - -	SPI3_NSS/I2S3_WS - USART1_RX	- - MDIOS_MDIO	SAI4_FS_B DCMI_D1 LCD_B1 EVENTOUT	
78	**LCD_BL**	PA15	DBTRGI **TIM2_CH1**/TIM2_ETR SAI4_D2 SDMMC1_CDIR	CEC SPI1_NSS/I2S1_WS SPI3_NSS/I2S3_WS SPI6_NSS	UART4_RTS/UART4_DE SDMMC2_D5 SDMMC2_CDIR SDMMC1_D5	SAI4_FS_A UART7_TX LCD_R1 EVENTOUT	
MISC							
79	LCD_R0 CSI_CKP LVDS1_CLKP	PH2	LPTIM1_IN2 - - -	- - - -	- QUADSPI_BK2_IO0 SAI2_SCK_B ETH1_GMII_CRS/ ETH1_MII_CRS	- - **LCD_R0** EVENTOUT	
80	LCD_G0 DSI_DP3 LVDS0_TX3P	PB1	- TIM1_CH3N TIM3_CH4 TIM8_CH3N	- DFSDM1_DATIN1 -	- LCD_R6 - ETH1_RGMII_RXD3	MDIOS_MDC - **LCD_G0** EVENTOUT	ADC1_INP5, ADC2_INP5
81	LCD_G1 DSI_DN3 LVDS0_TX3N	PE6	TRACED2 TIM1_BKIN2 SAI1_D1 -	TIM15_CH2 SPI4_MOSI SAI1_SD_A SDMMC2_D0	SDMMC1_D2 - SAI2_MCLK_B -	FMC_A22 DCMI_D7 **LCD_G1** EVENTOUT	
82	LCD_B0	PE4	TRACED1 - SAI1_D2 DFSDM1_DATIN3	TIM15_CH1N SPI4_NSS SAI1_FS_A SDMMC2_CKIN	SDMMC1_CKIN SDMMC2_D4 - SDMMC1_D4	FMC_A20 DCMI_D4 **LCD_B0** EVENTOUT	
MIPI-DSI							
83	**DSI_DP1** LVDS0_TX1P	DSI_DP1					
84	**DSI_DN1** LVDS0_TX1N	DSI_DN1					
85	**DSI_DP0** LVDS0_TX0P	DSI_DP0					
86	**DSI_DN0** LVDS0_TX0N	DSI_DN0					
87	**DSI_CKP** LVDS0_CLKP	DSI_CKP					
88	**DSI_CKN** LVDS0_CLKN	DSI_CKN					
UART							
89	UARTA_RXD	PB2	TRACED4 RTC_OUT2 SAI1_D1 DFSDM1_CKIN1	USART1_RX I2S_CKIN SAI1_SD_A SPI3_MOSI/I2S3_SDO	**UART4_RX** QUADSPI_CLK - -	- - - EVENTOUT	
90	UARTA_TXD	PG11	TRACED11 - - -	USART1_TX - **UART4_TX** -	SPDIFRX_IN0 - ETH1_RGMII_TX_CTL/ ETH1_RMII_TX_EN	- DCMI_D3 LCD_B3 EVENTOUT	
91	UARTB_RXD	PB12	- TIM1_BKIN I2C6_SMBA	I2C2_SMBA SPI2_NSS/I2S2_WS DFSDM1_DATIN1 USART3_CK	**USART3_RX** FDCAN2_RX - ETH1_R(G)MII_TXD0	- - UART5_RX EVENTOUT	
92	UARTB_TXD	PB10	- TIM2_CH3 - LPTIM2_IN1	I2C2_SCL SPI2_SCK/I2S2_CK DFSDM1_DATIN7 **USART3_TX**	QUADSPI_BK1_NCS - ETH1_(G)MII_RX_ER	- - LCD_G4 EVENTOUT	
93	UARTC_RXD	PD6	- TIM16_CH1N SAI1_D1 DFSDM1_CKIN4	DFSDM1_DATIN1 SPI3_MOSI/I2S3_SDO SAI1_SD_A **USART2_RX**	- - - -	FMC_NWAIT DCMI_D10 LCD_B2 EVENTOUT	
94	UARTC_TXD	PD5	- - - -	- - - **USART2_TX**	- - SDMMC3_D2 -	FMC_NWE - - EVENTOUT	
95	UARTC_CTS	PD3	HDP5 - - DFSDM1_CKOUT	- SPI2_SCK/I2S2_CK DFSDM1_DATIN0 **USART2_CTS**/ USART2_NSS	SDMMC1_D123DIR SDMMC2_D7 SDMMC2_D123DIR SDMMC1_D7	FMC_CLK DCMI_D5 LCD_G7 EVENTOUT	**Input** signal

PIN	QSCOM STANDARD	MP1 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks Additional functions
96	UARTC_RTS	PD4	- - - -	- SAI3_FS_A **USART2_RTS**/ USART2_DE	- - SDMMC3_D1 DFSDM1_CKIN0	FMC_NOE - - EVENTOUT	
2ⁿᵈ SPI							
97	SPIB_NSS	PZ3	- - I2C6_SDA I2C2_SDA	I2C5_SDA SPI1_NSS/I2S1_WS I2C4_SDA USART1_CTS/USART1_NSS	**SPI6_NSS** - - -	- - - EVENTOUT	
98	SPIB_MISO	PA6	- TIM1_BKIN TIM3_CH1 TIM8_BKIN	SAI4_CK2 SPI1_MISO/I2S1_SDI - -	**SPI6_MISO** TIM13_CH1 - MDIOS_MDC	SAI4_SCK_A DCMI_PIXCLK LCD_G2 EVENTOUT	ADC1_INP3, ADC2_INP3
99	SPIB_MOSI	PZ2	- - I2C6_SCL I2C2_SCL	I2C5_SMBA SPI1_MOSI/I2S1_SDO I2C4_SMBA USART1_TX	**SPI6_MOSI** - - -	- - - EVENTOUT	
100	SPIB_SCK	PA5	- TIM2_CH1/TIM2_ETR - TIM8_CH1N	SAI4_CK1 SPI1_SCK/I2S1_CK - -	**SPI6_SCK** - - -	SAI4_MCLK_A - LCD_R4 EVENTOUT	ADC1_INP19, ADC1_INN18, ADC2_INP19, ADC2_INN18, DAC_OUT2

Onboard wiring

	Pins used for manufacturing and debugging – leave unconnected				
PIN	(MP1 PAD NAME)	**PIN**	(MP1 PAD NAME)	**PIN**	(MP1 PAD NAME)
C1	**JTAG_TDI** (JTDI)			C3	**JTAG_TCK** (JTCK-SWCLK)
		B2	**JTAG_TDO** (JTDO-TRACESWO)		
A1	**JTAG_TRST_B** (NJTRST)			A3	**JTAG_TMS** (JTMS-SWDIO)

PIN	USED FOR	MP1 PAD	Alternate Function 0-3	Alternate Function 4-7	Alternate Function 8-11	Alternate Function 12-15	Remarks
Onboard peripherals wiring							
	SERIAL FLASH	PB6 10K-PU	- TIM16_CH1N TIM4_CH1 -	I2C1_SCL CEC I2C4_SCL USART1_TX	- FDCAN2_TX **QUADSPI_BK1_NCS** DFSDM1_DATIN5	UART5_TX DCMI_D5 - EVENTOUT	
		PF10 10K-PU	- TIM16_BKIN SAI1_D3 SAI4_D4	- - SAI1_D4 -	- **QUADSPI_CLK** - -	SAI4_D3 DCMI_D11 **LCD_DE** EVENTOUT	
		PF8 10K-PU	TRACED12 TIM16_CH1N - -	- SPI5_MISO SAI1_SCK_B UART7_RTS/UART7_DE	- TIM13_CH1 **QUADSPI_BK1_IO0** -	- - - EVENTOUT	
		PF9 10K-PU	TRACED13 TIM17_CH1N - -	- SPI5_MOSI SAI1_FS_B UART7_CTS	- TIM14_CH1 **QUADSPI_BK1_IO1** -	- - - EVENTOUT	
	eMMC	PG6 10K-PU	TRACED14 TIM17_BKIN - -	- - - -	- - **SDMMC2_CMD** -	- DCMI_D12 LCD_R7 EVENTOUT	
		PE3 10K-PU	TRACED0 - - -	TIM15_BKIN - SAI1_SD_B -	- **SDMMC2_CK** - -	FMC_A19 - - EVENTOUT	
		PB14 10K-PU	- TIM1_CH2N TIM12_CH1 TIM8_CH2N	USART1_TX SPI2_MISO/I2S2_SDI DFSDM1_DATIN2 USART3_RTS/USART3_DE	- **SDMMC2_D0** - -	- - - EVENTOUT	
		PB15	RTC_REFIN TIM1_CH3N TIM12_CH2 TIM8_CH3N	USART1_RX SPI2_MOSI/I2S2_SDO DFSDM1_CKIN2 -	- **SDMMC2_D1** - -	- - - EVENTOUT	
		PB3	TRACED9 TIM2_CH2 - -	SAI4_CK1 SPI1_SCK/I2S1_CK SPI3_SCK/I2S3_CK -	SPI6_SCK **SDMMC2_D2** - -	SAI4_MCLK_A UART7_RX - EVENTOUT	
		PB4	TRACED8 TIM16_BKIN TIM3_CH1 -	SAI4_CK2 SPI1_MISO/I2S1_SDI SPI3_MISO/I2S3_SDI SPI2_NSS/I2S2_WS	SPI6_MISO **SDMMC2_D3** - -	SAI4_SCK_A UART7_TX - EVENTOUT	
		PA8	MCO1 TIM1_CH1 TIM8_BKIN2	I2C3_SCL SPI3_MOSI/I2S3_SDO USART1_CK	SDMMC2_CKIN **SDMMC2_D4** OTG_FS_SOF/OTG_HS_SOF 	SAI4_SD_B UART7_RX LCD_R6 EVENTOUT	
		PB9	HDP7 TIM17_CH1 TIM4_CH4 DFSDM1_DATIN7	I2C1_SDA SPI2_NSS/I2S2_WS I2C4_SDA SDMMC2_CDIR	UART4_TX FDCAN1_TX **SDMMC2_D5** SDMMC1_CDIR	SDMMC1_D5 DCMI_D7 LCD_B7 EVENTOUT	
		PC6	HDP1 - TIM3_CH1 TIM8_CH1	DFSDM1_CKIN3 I2S2_MCK - USART6_TX	SDMMC1_D0DIR SDMMC2_D0DIR **SDMMC2_D6** DSI_TE	SDMMC1_D6 DCMI_D0 LCD_HSYNC EVENTOUT	
		PC7	HDP4 - TIM3_CH2 TIM8_CH2	DFSDM1_DATIN3 - I2S3_MCK USART6_RX	SDMMC1_D123DIR SDMMC2_D123DIR **SDMMC2_D7** -	SDMMC1_D7 DCMI_D1 LCD_G6 EVENTOUT	
	LED	PA13					Low: LED on

Electrical characteristics

Absolute maximum ratings

Parameter	Symbol	Min	Max	Remarks
Power supply	VIN	0V	3.9V	
Input voltage on USB VBUS pins	USBA_VBUS USBB_VBUS	0V	6V	
Input voltage on USB DN/DP pins	USBA_DN/DP USBB_DN/DP	0V	5.5V	
Input voltage on any other pins		0V	3.9V	
Storage temperature range	$T_{STORAGE}$	-40°C	150°C	Version without eMMC
		-40°C	85°C	Version with eMMC

Operating ranges

Parameter	Symbol	Min	Max	Remarks
Power supply	VIN	3.1V	3.6V	
I/O input low level voltage	V_{IL}	-	0.3 x VIN	
I/O input high level voltage	V_{IH}	0.7 x VIN	-	
I/O output voltage	Refer to STM32MP1 datasheet, chap. Output voltage levels.			VDD=VIN=3.3V typ.
Operating temperature range	T_{AMB}	-25°C -40°C	85°C	QSMP /E85 QSMP /I
Processor junction temperature	T_J	-40°C	125°C	

Power supply currents

Parameter	Symbol	VIN	Current	Remarks
At U-Boot prompt	I_{UBOOT}	3.3V	195mA	
At Linux prompt	I_{LINUX}	3.3V	TBD	All pins left unconnected
Sleep	I_{SLEEP}	3.3V	TBD	
Maximum calculated	I_{MAX}	3.3V	700mA	Calculated on max. IDD's @ 80% onboard power supply efficiency.
Power supply rating	I_{SUPP}	3.3V	1A	With margin for sizing the power supply

Alternate UART pin mappings

	RX	TX	RTS/DE	CTS/NSS	CK	Remarks
USART1	9, 36, 77, 89	21, 90, 99	6	5, 97	8	
USART2	**93**	22, **94**	24, **96**	16, 63, **95**	19	
USART3	30, 41, **91**	42, 76, **92**	7	14, 15, 55	39, 72, 91	
UART4	5, 11, 24, 32, 40, 41, 54, 65, **89**	6, 12, 16, 38, 42, 64, **90**	78	28		
UART5	13, 40, 91	14, 39	38	37		
USART6		34	70	35	1, 38, 56	
UART7		78				
UART8			3, 56	63, 71		

Alternate function mappings

#	USART1	USART2	USART3	UART4	UART5	USART6	UART7	UART8	TIM1	TIM2	TIM3	TIM4	TIM5	TIM8	TIM12	TIM13	TIM14	TIM15	TIM16	TIM17	SPI1	SPI2	SPI3	SPI4	SPI6	SAI1	SAI2	SAI3	SAI4	MMC1	FDCAN1	FDCAN2	I2C1	I2C2	I2C3	I2C4	I2C5	I2C6
1						CK			CH2															NSS			SD_B											
2									CH1									CH1						MISO	CK2					D0DIR								
3								RTS	CH4															MOSI			MCLKB			DIR								
4																								SCK	CK1											SCL		
5	CTS			RX					CH4													NSS									RX						SCL	SCL
6	RTS			TX					ETR																		FS_B				TX						SDA	SDA
7			RTS						IN1	IN1		CH1															FS_A								SCL		SCL	
8	CK																					SCK			SCK										SCL			SCL
9	RX																					MISO			MISO											SDA	SDA	SDA
10																																	SDA			SDA		
11				RX																						SCK_A					RX						SDA	SDA
12				TX																						SD_A					TX						SCL	SCL
13					RX				BKIN		CH2										BKIN	MOSI		MOSI	MOSI		D1				RX		SMBA			SMBA		
14			CTS	TX					CH1N	OUT														SCK								TX						
15			CTS								IN2																SD_A						SMBA			SMBA		
16		CTS		TX					BKIN		CH1		CH1	ETR				BKIN									SD_B											
17									OUT			CH2	CH3															SCK_A								SDA		SDA
18													CH3															FS_A										
19		CK											ETR								NSS		NSS		NSS			D2										
20									ETR																													
21	TX								CH2													SCK														SMBA		
22		TX							CH1	CH3		OUT	CH3					CH1										SCKB										
23																							MOSI						D1									
24		RTS		RX					CH1N	CH2	OUT	CH2			CH1N													MCLKB				TX						
25									CH1N		CH2		CH1N	CH1								MOSI			MOSI			D1										
26																																						
27																											D3		D4									
28			CTS						CH2N		CH3		CH2N																									
29																																					SCL	
30		RX									CH4																										SDA	
31									BKIN2																													
32				RX					_CH1		CH3							CH1												CKIN	RX		SCL			SCL		
33																								MISO														
34				TX					ETR															MOSI					D1									
35					CTS				OUT															SCK	CK2				CK1									
36	RX								_CH1N		CH2				CH1N																					SDA		SDA
37					CTS						CH4		CH4																D1							SDA		
38		TX	RTS			CK					CH3		CH3																	D0								
39		CK		TX																					MOSI				D3	CK								
40				RX	RX							ETR																		CMD								SMBA
41		RX	RX																				MISO						SCK_B	D3								
42		TX	TX																						SCK				MCLKB	D2								

Pin	USART1	USART2	USART3	UART4	UART5	USART6	UART7	UART8	TIM1	TIM2	TIM3	TIM4	TIM5	TIM8	TIM12	TIM13	TIM14	TIM15	TIM16	TIM17	SPI1	SPI2	SPI3	SPI4	SPI6	SAI1	SAI2	SAI3	SAI4	MMC1	FDCAN1	FDCAN2	I2C1	I2C2	I2C3	I2C4	I2C5	I2C6
53									CH3															MISO			FS_B											
54				RX																											RX							
55			CTS																																			
56						CK		RTS																		MCLKA												
57																											MCLKB											
58													ETR																							SDA		
59									CH2						CH2																					SMBA		
60													CH1																				SMBA			SMBA		
61													CH2																				SCL			SCL		
62													CH3																				SDA			SDA		
63		CTS					CTS		BKIN									BKIN																				
64				TX										CH1N																	TX							
65				RX										CH2N																	RX							
66														CH3N																								
67													CH4									NSS																
68														BKIN2								SCK																
69														CH4							MISO																	
70						RTS			IN1															MISO					CK2									
71								CTS																				SD_B										
72			CK						BKIN							BKIN							MISO				FS_B											SMBA
73														BKIN													MCLKA											
74														CH1													SCK_A											
75														CH2													SD_A											
76		TX																										SCK_B										
77	RX								CH3															NSS				FS_B										
78				RTS			TX		CH1													NSS		NSS	NSS				D2	CDIR								
79									IN2																			SCK_B										
80									CH3N		CH4			CH3N																								
81									BKIN2									CH2					MOSI				D1	MCLKB		D2								
82									CH1N									CH1N						NSS					D2	CKIN								
89	RX			RX																		MOSI							D1									
90	TX			TX																																		
91			CK		RX				BKIN													NSS										RX		SMBA				SMBA
92			TX							CH3												SCK												SCL				
93		RX							CH1N									CH1N				MOSI						D1										
94		TX																																				
95		CTS																				SCK								DIR								
96		RTS																									FS_A											
97	CTS																				NSS			NSS											SDA	SDA	SDA	SDA
98									BKIN		CH1			BKIN	CH1							MISO			MISO				CK2									
99	TX																					MOSI			MOSI										SCL	SMBA	SMBA	SCL
100										CH1				CH1N								SCK			SCK				CK1									